LOW-COST TEST, DIAGNOSIS, AND TUNING FOR ADAPTIVE RADIO FREQUENCY SYSTEMS

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Dedicated to my loving parents...

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LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
ADSL	Asymmetric Digital Subscriber Loop
AGC	Automatic Gain Control
ATE	Automatic Test Equipment
BER	Bit Error Rate
BERT	Bit Error Rate Tester
BIST	Built-In Self-Test
BIT	Built-In Test
BPSK	Binary Phase Shift Keying
CCDF	Cumulative Complimentary Distribution function
CDMA	Code Division Multiple Access
CMOS	Complimentary Metal Oxide Semiconductor
CP	Cyclic Prefix
DAB	Digital Audio Broadcast
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DC	Direct Current
DFT	Design for Testability
DSP	Digital Signal Processing

DS-UWB	Direct Sequence Ultra Wide Band
DUT	Device Under Test
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FDM	Frequency Division Multiplexing
FFT	Fat Fourier Transform
FSK	Frequency Shift Keying
GSM	Global System for Mobile Communications
I	In Phase
IFFT	Inverse Fast Fourier Transform
IIP3	Input third-order Intercept
ISI	Inter-Symbol Interference
ITRS	International Technology Roadmap for Semiconductor
LMS	Least Mean Square
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass filter
LS	Least Squares
LSB	Least Significant Bit
LUT	Look-Up table
MAC	Media Access Control
MARS	Multivariate Adaptive Regression Splines
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing

MCML	Metal Oxide Semiconductor Current Mode Logic
NF	Noise Figure
OFDM	Orthogonal frequency Division Multiplexing
PA	Power Amplifier
PAR	Peak-to-Average Ratio
PCB	Printed Circuit Board
PCS	Public Communication System
PPM	Pulse Position Modulation
PSD	Power Spectral Density
PSK	Phase Shift Keying
Q	Quadrature
QAM	Quadrature Amplitude Modulation
QOS	Quality of Service
QPSK	Quadrature Phase shift Keying
RF	Radio Frequency
RFID	Radio Frequency Identification
RLC	Radio Link Control
RLS	Recursive Least Squares
RMS	Root Mean Square
SDR	Software Defined Radio
SIA	Semiconductor Industry association
SNR	Signal-to-Noise Ratio
TFC	Time Frequency Code

TDMA	Time Division Multiple Access
TH-UWB	Time Hopping Ultra Wide Band
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

SUMMARY

The continuing trend of miniaturization in semiconductor devices has enabled the integration of complex functionalities on-chip, leading to a proliferation of wireless devices for both mobile and in-office applications. The use of scaled CMOS technologies for high-frequency wireless devices is posing daunting technological challenges, both in the design and post-manufacture testing of such devices. Circuits are becoming increasingly susceptible to manufacturing process variations, device wear-out phenomena, and coupled noise from substrate and power planes. This leads to loss of manufacturing yield and operational reliability in field. The use of techniques that enable thorough testing and tuning of these RF systems to make them resilient to the above-mentioned factors are, therefore, becoming critical in the development of such devices. The issue of device power consumption and heat dissipation is also dominating future wireless transceiver designs. This is driven by the trend of increasing operating speeds coupled with dense integration of multi-mode functionalities onto compact form-factors on-chip.

To enable reliable operation of systems, they should first be tested for performance compliance, and diagnosed for any non-idealities. Appropriate tuning must then be performed to restore system performance above pre-defined threshold levels. The approaches adopted should be low-cost with minimal hardware or software overhead to ensure that the final product meets the requirements of economics in the market place. For enabling low-power operation of a wireless device under changing environmental conditions, aggressive design techniques that dynamically adapt the

system for reduced power consumption across temporally varying conditions should be developed.

In this thesis, a framework for reliable low-power operation of wireless devices is presented. This framework uses low-cost test, diagnosis, and tuning techniques. As illustrated in Figure 1, two main approaches are utilized to address the issue. The first approach is offline, where the device is tested and compensated for any performance loss during post-manufacture production testing. To do this, each device in the production line is tested using automatic test equipment (ATE) for correct operation, and diagnostic parameters required for adequate tuning are extracted. In the concurrent approach, the RF devices are dynamically tested in the field to monitor the performance. In addition to RF sensors deployed in the front-end, transmitter-receiver loopback techniques are used to test system and extract appropriate diagnostic information that is fed to the on-board digital signal processor (DSP). Appropriate tuning is then performed using control signals from the on-board DSP. The proposed approach not only increases the reliability of the device, but also enables the operation at the minimum power consumption. Low-power operation is achieved through continuous tuning of device tuning 'knobs' based on a multi-dimensional control law running on the DSP. During online operation, the control law operates the system at the lowest power consumption levels under all environmental conditions. This adaptation is performed continuously while ensuring that system-level performance metrics are never violated. This approach has direct implications for boosting the battery life of portable wireless devices while ensuring their operational reliability.

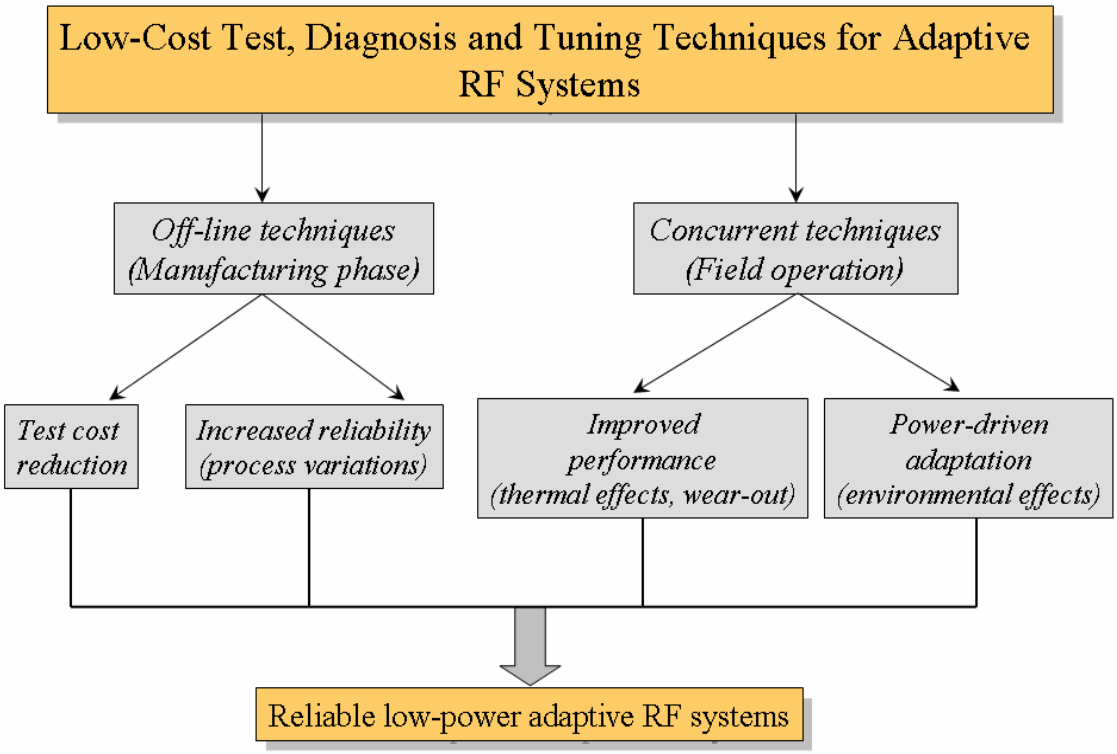


Figure 1. Proposed low-cost test, diagnosis, and tuning framework for reliable low power operation of adaptive RF systems

Chapter 1

INTRODUCTION

Wireless communication for both mobile and in-office applications is undergoing a revolution as a result of the proliferation of different communication standards spanning diverse communication bandwidths. The use of scaled complimentary metal oxide semiconductor (CMOS) technologies for high frequency wireless technologies is posing daunting technological challenges in development of such devices. Technology scaling has been accompanied by increased performance and power sensitivity to process variations [1][2]. Figure 2 shows the current trends of 3σ process variations for three representative parameters in which process variations have increased with the reduction in transistor feature sizes. Circuits are becoming increasingly susceptible to manufacturing process variations resulting in a reduction in manufacturing yield. As a result, testing the system for correct functionality, diagnosis of parameters, and performing compensation will be crucial in the development of such devices. As shown in Figure 3, the test cost trend was predicted in the 1997 semiconductor industry association (SIA) roadmap in which test capital per transistor was expected to exceed the silicon capital cost.

New approaches must be developed to address the challenges keeping in mind the increasing levels of complexity and more importantly, the need for a low-cost solution. The ability to perform low-cost testing is a key factor that determines the

overall manufacturing cost [3]-[7] of devices, and minimizing it is crucial to success at the market place. Once the device is tested, compensation or tuning of the system must be performed to improve the performance and also improve the manufacturing yield. Apart from the post-manufacture production testing and compensation, in-field testing and tuning while the device is in operation is also important to ensure that the device is robust to environmental variations. There is increasing pressure on the manufacturers to develop low-cost reliable wireless devices. In this respect, the issue of device power consumption and heat dissipation is also dominating future designs. This is due to enhanced data processing capability of wireless consumer devices enabling multiple applications to be run on these devices. Developing aggressive low-power techniques that fully exploit the design margins of the system and adaptively operate the device at optimum power under different operating conditions have, therefore, become important.

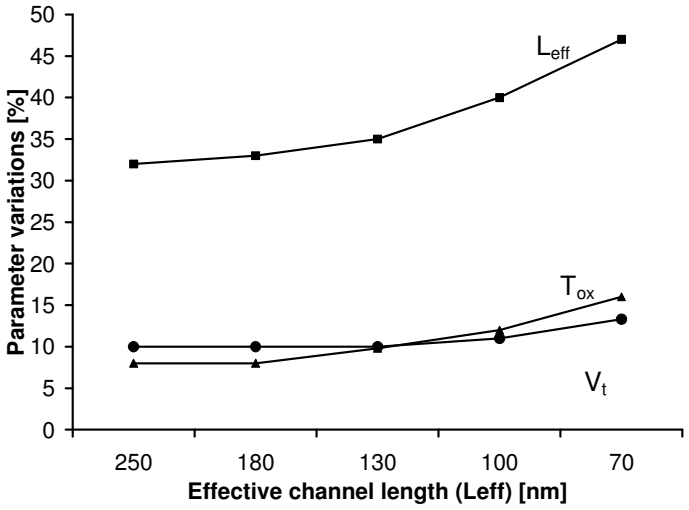


Figure 2 Technology parameter 3σ variations [2].

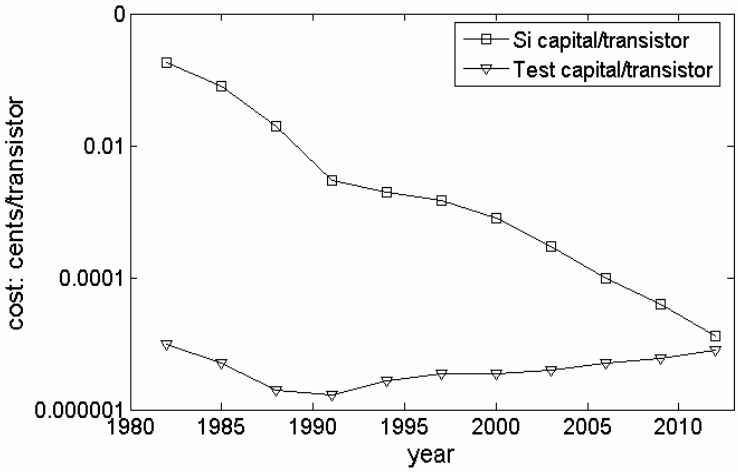


Figure 3 Silicon and test capital trends.

1.1 WIRELESS TRANSCEIVER TESTING

The production test of wireless transceivers is done in two phases, wafer-level test and final test. Wafer-level test is performed on fabricated wafers to prevent bad dies from being passed through further production steps. Final test is performed on the packaged wafers to guarantee performance of the device at the end of the production line. The devices are tested for various baseband or radio frequency (RF) system specifications. The wireless transceivers are usually implemented as two- or three-chip solutions, comprising of baseband and RF modules. The interface between the RF and baseband part that is available for test is an analog in-phase (I) and a quadrature (Q) link. The specifications usually tested at this link include direct current (DC) offset, magnitude and phase of I and Q signals and phase noise. The other standard circuit-level specifications for wireless devices/systems during high-volume tests are the gain, the 1-dB compression point, the harmonic distortion, the third-order input intercept point (IIP3), the adjacent channel power ratio (ACPR), the noise figure (NF), and phase noise. Most of the specifications involve power measurements at the input and output pins of a

device under test (DUT) and characterizing the harmonic components. Though measuring these specifications has some advantages like providing the ability to characterize individual functional blocks, increasing integration and migration towards a single chip solution has made these traditional metrics less useful. System-level specifications like error vector magnitude (EVM) and bit error rate (BER) offer a convenient way to test these devices at the system-level providing a more meaningful test data [8][11]. They capture the overall effect of all the non-idealities in the transceiver including analog-to-digital converter (ADC) and digital-to-analog converter (DAC) non-linearities, sampling clock jitter, RF-front non-linearity, gain variations, local oscillator (LO) frequency offset, and phase noise etc.

EVM and BER are two common system-level specifications that determine the performance of the wireless device in terms of transmitted and received symbols. These tests are performed by capturing the response of the wireless system at baseband symbol rate (at speed). Measuring the EVM and BER of a system in lieu of individual RF and baseband circuit specifications is convenient and quantifies the overall transceiver performance. EVM quantifies the difference (error vector) between the transmitted and received symbols at the baseband as shown in Figure 4. It is computed as

$$EVM = \sqrt{\frac{1}{N}\frac{\sum_{1}^{N}\|y_i - x_i\|^2}{\|y_{\max}\|^2}}, \qquad (1)$$

where y_i is the received complex data, x_i is transmitted complex data, y_{max} is the outermost data point in the constellation diagram and, N is the number of complex data points used for computation, where N is sufficiently large. It computes the root mean square (RMS) of the error vector magnitudes of N transmit-receive pairs expressed as

percentage of reference data-vector amplitude. Typically, a large number of symbols need to be transmitted and received to determine the EVM value. The above definition of EVM is general and is applicable to both single and multiple-carrier systems. It provides a simple and useful metric for measuring the quality of digitally modulated signals. It is integrated into several existing and upcoming communication standards.

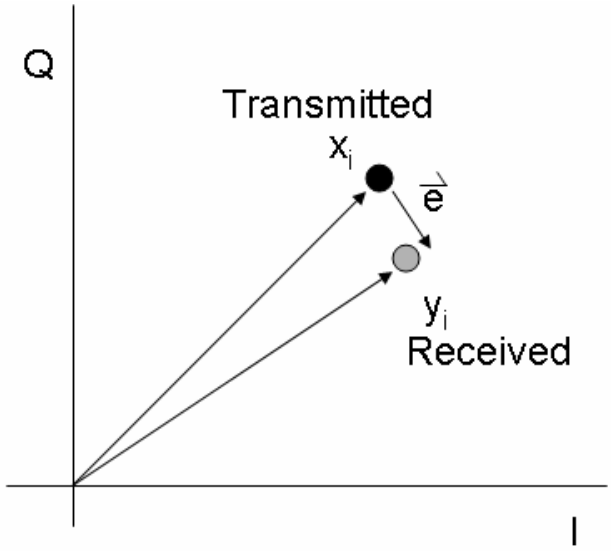


Figure 4 Error between transmitted and received symbols. EVM is computed by taking the RMS of the error vectors

BER denotes the probability of a received bit being incorrect in presence of system non-idealities. Channel effects viz. multi-path, frequency selective fading, etc. are not usually considered for measuring BER under production test. This is done to ensure repeatability in the obtained results during production test. The BER is formulated as

$$BER = \frac{N_e}{N_{tx}} = \frac{e(t_p)}{R \times t_p}, \qquad (2)$$

where t_p is the measurement period, R is bit rate, N_e is the number of error bits and, and N_{tx} is the number of bits transmitted. BER testing of wireless devices in production test

also involves transmitting a large number of bits from a BER Tester (BERT), passing the bits through the RF front-end system, and receiving the bits in the BERT or the receive section of the device under test (DUT). Finally, analysis is performed using the above equation to obtain the BER for the system. The BERT can transmit different patterns, introduce various errors (delay and jitter), and compensate for cable effects.

1.1.1 Previous Research Efforts to Lower Test Cost of Wireless Circuits/ Transceivers

Production testing of RF transceiver devices traditionally involves breaking down the larger problem into several smaller problems by testing individual components or subsystems separately. For example, testing baseband processor is done primarily by means of the IEEE 1149.1 boundary scan [12], and testing analog subsystems is done by means of inserting additional test accesses around it [13][14][15]. However, for testing embedded RF components, putting additional test accesses is not favored because of the adverse effect of these access points on impedance matching. Built-in self test (BIST) approaches for RF devices and systems have been explored in the past. Though BIST is used widely in digital systems, its applicability to RF systems is not well understood. The work presented in [16] measures the spectral content of the test response using the direct down-conversion of RF test stimuli and test response waveforms. Although the chip area taken by additional test circuitry is of concern, it shows the feasibility of using a built-in test for measuring the performance of high-frequency embedded analog/RF blocks in-situ. The authors of [17] have developed a sub-sampling-based digitizer that can be used for capturing narrow-band RF waveforms. On the other hand, in [18], the authors attempt to extend their delta-sigma modulator-based built-in self-test (BIST)

approach for measuring signal-to-noise ratio (SNR), frequency response, and intermodulation effects for wireless communication devices. A conceptual down-conversion path on the same chip for down-converting the transmitter output back to baseband for ease of testing was proposed in [19]. A BIST approach was presented in [20] that uses the baseband processor for EVM computation. While the BIST approach is very attractive for reducing the test cost, its large-scale practical applicability in RF circuits is many years away.

A defect-oriented testing approach and the corresponding concept of fault coverage in test automation for testing Bluetooth transceivers was presented in [21][22]. For system-level baseband specifications, such as BER [23][24][27] and EVM [25][26], analysis pertaining to different data modulation schemes have been analyzed in the past. An accelerated measurement technique has been tried for lowering the test time for digital data links [28][29]. An approach to reduce the EVM computation time on production testers for global system for mobile communications (GSM) applications is discussed in [30]. The test time is reduced by more than an order of magnitude by avoiding tedious matrix inversion operations that are usually required to compute EVM In [31], the automation of EVM measurement for quadrature amplitude modulation (QAM) devices is discussed. *'Alternate'* test techniques are employed in [32] to test for system-level specifications of RF transceivers using low-cost signal sources. The problem of bandwidth limitation of ATE cable is alleviated by designing a modulator that up-converts the low-frequency test signal sent from ATE, and a demodulator that down-converts the RF test response to low frequency on the DUT load-board.

'Alternate' testing has been applied to perform specification testing of analog and RF components and circuits in the past [32]-[36]. They were employed also to test for system-level specifications of RF transceivers using low-cost signal sources. To perform parametric specification testing of devices, the use of a defect filter to screen out defective parts (catastrophic faults) was assumed. Multiple system specifications are predicted from the test response of the DUT to a carefully crafted test stimulus as illustrated in Figure 5. The prediction accuracy of alternate test depends on the test conditions and devices training data set. In [37], the author attempted to replace the need for using high-frequency testing by alternately monitoring the transient change in the bias current of an RF time-domain multiplexing access (TDMA) power amplifier, and the information contained in such changes in bias current is measured to be reflective of DUT specifications, such as ACPR [38].

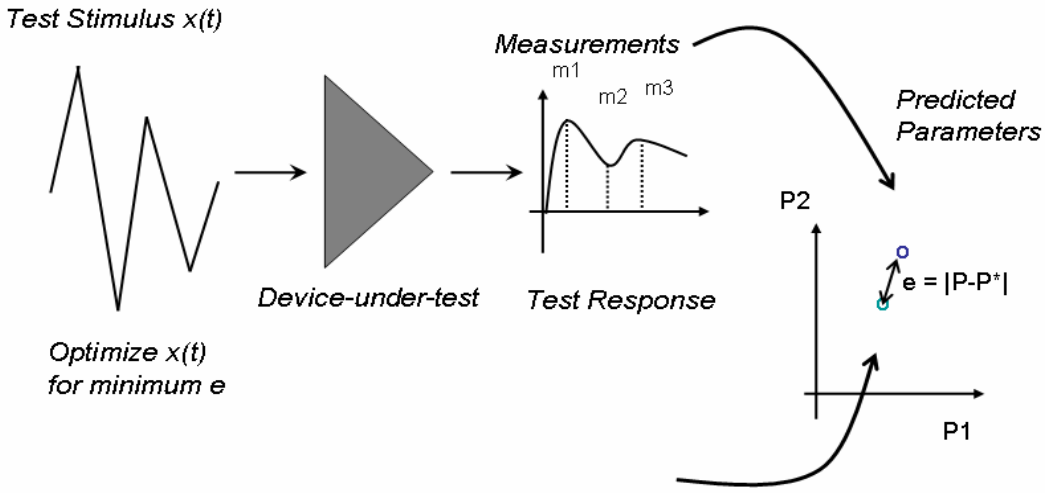


Figure 5 Alternate test flow

With increasingly complex modulation schemes being used in communication systems, and considering the complex radios of the future (like software-defined radio

architectures (SDR)), significant research is needed towards efficient and cost-effective production test techniques. In this thesis, novel test techniques are developed for lowering test-time and test-cost of ultra-wide band (UWB) transceivers and orthogonal frequency division multiplexing (OFDM) systems. Apart from post-manufacture production testing, low-cost test techniques for online/concurrent diagnosis and compensation of radios need to be developed to ensure reliable operation of these systems. The following section discusses the importance of diagnosis and tuning in RF transceivers, and the work that has been done so far in this area.

1.2 NON-IDEALITIES IN WIRELESS TRANSCEIVERS: DIAGNOSIS AND COMPENSATION

The overall performance of an RF transceiver is dependent on the operation of individual subsystems that comprise the transceiver. The RF and analog blocks in a transceiver system may exhibit non-idealities due to process variations and device mismatches. Deviations in performance result in the loss of manufacturing yield, and affect the operational reliability of circuits in the field. Further, continually changing environmental conditions including temperature and aging affect the performance of these systems. The resulting degradation of performance may result in a total loss of communication, or result in a lower throughput making the system error-prone. Designing the system with a conservative analysis of the front-end requirements for compliance with [39][40] leads to severe, over-dimensioned specifications[41][42]. Such a conservative design would not meet the requirements of economics in the market place, i.e. low cost and low power consumption requirements. Often, the design of the front-end is oriented towards lower power consumption and reducing manufacturing cost

which, in return reduces the performance of the systems. Systems engineers deal with the lower RF front-end performance by using some compensation schemes at the system- or circuit-level. Compensation techniques that address these shortcomings in the analog and RF subsystems have attracted much attention, and significant work has been done in this area. One way of classifying the compensation techniques published in literature is - digital or analog. In the digital approach, the compensation for the RF front-end non-idealities is performed digitally in the baseband processor. This type of compensation is effective, needs little or no overhead, and is broader in scope when compared to analog techniques.

The non-idealities present in wireless communication system may occur in the RF front-end, baseband or digital stage. The RF portion in wireless transceivers suffers from signal saturation, nonlinear distortion, and DC offset. The baseband stage on the other hand suffers from I/Q gain mismatch, I/Q phase mismatch and DC offset. In direct-conversion receivers, all the above mentioned effects are collectively referred to as front-end non-idealities. In analog compensation, the compensation is performed in the analog domain by modifying circuit characteristics such as bias, supply voltage etc [43]-[47]. Compensation for temperature effects using band-gap bias circuits and gain variations using automatic gain control circuits (AGCs) are widely used. But, analog compensation techniques, in general suffer from many limitations that include inefficiency, due to lack of sufficient control, significant area overhead, and higher power consumption. Digital compensation, on the other hand uses digital signal processing (DSP) algorithms running in the baseband processor to correct for and calibrate-out the effects of various non-idealities discussed above[48]-[54].

Techniques adopted for digital compensation of transceiver systems can in general be classified as adaptive [48]- [53], or non-adaptive [54]. Adaptive compensation is usually performed through continuous online monitoring, and calibrating the system using search techniques like least squares (LS), least mean squares (LMS) or recursive least squares (RLS). In non-adaptive compensation, a one-time calibration of the system is done during production test. Each DUT in the production line is tested and calibrated 'on-the-fly' using digital control signals from the ATE. To enable this, high-performance RF test equipment is required, which increases the manufacturing test cost. Another drawback of this approach is its inability to track and compensate for variations *in the field* caused by temperature drift and device wear-out etc. Due to the above mentioned reasons, adaptive online compensation is usually performed. But, adaptive compensation techniques also suffer from certain deficiencies. In a system that suffers from significant deviations in performance due to multiple effects, compensation is difficult and sensitive to inaccuracies. Moreover, the compensation technique would a large number of iterations for convergence, or in some cases, may not converge at all. The papers published in literature usually consider non-idealities in isolation, and propose adaptive schemes that tackle these isolated effects. Such schemes may not be very effective in a system that simultaneously suffers from multiple effects such as frequency offset, phase noise, non-linearity etc. Adaptive techniques that co-optimize the wireless transceiver for low-power, while simultaneously compensating for non-idealities have not been studied. In the proposed approach, a concurrent diagnostic testing and compensation technique for wireless transceivers that co-tunes analog/digital parameters for performance compensation under performance variations is proposed. The proposed approach also

constantly strives to operate the transceiver at minimum power consumption levels while simultaneously performing compensation. This has direct implications for boosting the battery life of portable wireless devices.

1.3 POWER CONSUMPTION ISSUES IN WIRELESS DEVICES

Several techniques for low power operation of circuits have been proposed in the literature [55]-[72]. Broadly, they are classified as circuit-level (physical layer) techniques and higher-level wireless protocol-based techniques. At the physical layer, low-power design methodologies for digital systems have been studied extensively [55][57], but relatively fewer techniques have been proposed for RF systems. Some of the design techniques proposed for power minimization in RF circuits include bias current reuse [60], functional combination [61], controlled positive feedback [62], high impedance interfaces [63] and sub threshold biasing [64]. In future systems, there is a need for co-optimizing RF front-end and baseband power consumption metrics as the devices become more complex and power hungry [59][65][67]. The broader issue with present physical layer design techniques is that design margins are incorporated into the circuits to account for *worst-case* estimates of process variability, and thermal effects in the RF front-end, and channel conditions. However, for a significant portion of the time a wireless device is powered up for operation, it *is not in a worst case environment.* Hence, the circuit operation is not optimal from a power consumption standpoint under the majority of operating conditions. There also exist media access layer (MAC) and network-level dynamic power management schemes [68] that strive to conserve power by adapting the data rate (modulation and coding rates) based on certain channel quality metrics derived from the analysis of training symbols. Training symbols are short bit

sequences that are transmitted prior to the data to ascertain the channel, and to calibrate the receiver for current channel conditions. Present-day wireless devices also feature high-power, low-power or shut-down modes, that are correspondingly exercised depending on the prevailing operating conditions. Though these approaches are effective in reducing the power consumption levels, they do so in a few discrete steps, and hence do not fully exploit the built-in design margins for lowest power operation while satisfying performance requirements.

To satisfy the demands for future generation of wireless systems, aggressive power management strategies should be employed at the *system-level* that adapts not only the RF and digital circuits, but also takes into account end-to-end cross layer interactions. In [72], an energy scalable RF transmitter was proposed, where the front-end is dynamically tuned (supply, bias, resistances) for each data rate modulation set by the higher-level link layer protocol. The effectiveness of the approach described in [72] depends on the accuracy of channel estimation procedure, and the pre-set transmitter calibration coefficients obtained during the design phase. In [69][70][71], the need for a co-design strategy comprising communication algorithms, protocols and digital architectures as well as analog and digital circuits is proposed. By using multi-dimensional optimization early in the design phase, a wireless device can designed to operate at significantly lower power consumption levels.

In this work, a novel approach for a dynamically tunable RF front-end that tunes the circuitry based on feedback from an adaptation metric. The adaptation metric is a system-level specification that is computed by the baseband signal processor in real-time (online). When this adaptation metric has a “high” value (high fidelity of the received

signal) the quality of signal processing in the RF front end (i.e. its performance) can be degraded intentionally by reducing its supply and bias voltages dynamically to save power while maintaining system-level performance metrics.

1.4 SUMMARY OF CONTRIBUTION OF THIS THESIS

In this thesis, a framework for reliable low-power operation for adaptive RF systems is presented. The framework uses low-cost test, diagnosis and tuning techniques during the manufacturing phase to drive down production test costs and increase the reliability of manufactured devices. During field operation of the wireless device, a test-enabled tuning approach is used to operate the system at low power consumption levels across temporally varying environmental conditions. The key contributions of this thesis are as follows.

- To reduce production test costs, a test technique that reduces the test time for EVM specification of a wireless OFDM device is developed. Besides test time reduction, the proposed approach also allows the use of low-cost instrumentation for performing production test. The proposed method can also be used for accurate characterization of system noise.
- BER test time reduction techniques are developed for digitally modulated wireless systems such as OFDM and MB-OFDM UWB devices, and pulse-based UWB systems.
- Test-enabled diagnosis and tuning methodology for RF systems is presented. In this approach, RF systems are tested by leveraging the functionality of the on-board ADC and DSP. The test is performed through deployment of test sensors in the transmitter to capture the test response. Alternately, transmitter-receiver

loopback is also used for test and diagnosis purposes. This work targets OFDM, multiband-OFDM (MB-OFDM) and phase/frequency modulated systems.

- A test-enabled multi-dimensional adaptive power management approach that optimally trades-off power vs. performance in wireless systems is developed. The control law operates the system at minimum power consumption levels across temporally changing operating conditions by concurrently tuning control parameters in the RF and digital baseband components of a wireless receiver.

This rest of this thesis is organized as follows. Chapter 2 discusses the proposed test approaches for EVM and BER specifications of wireless devices. The targeted schemes include OFDM and pulse-based UWB systems. In Chapter 3, the diagnosis and tuning approaches for RF systems are presented. Chapter 4 discusses the proposed multi-dimensional adaptive control scheme for low power operation of wireless devices. Finally, Chapter 5 summarizes the work with suggestions for future research.

Chapter 2

LOW-COST SYSTEM-LEVEL SPECIFICATION TESTING OF RADIO FREQUENCY TRANSCEIVERS

Low-cost test methodologies for orthogonal frequency division multiplexing (OFDM) devices and ultra-wide band (UWB) devices are presented in this chapter. The proposed techniques presented enable the testing of wireless transceivers using low-cost signal sources, and reduce the time required to test these devices. The targeted specifications are the system-level metrics – EVM and BER. Orthogonal frequency division multiplexing (OFDM) and ultra-wide band (UWB) pulse-based transceivers are used to validate the proposed approach. OFDM is a popular modulation scheme in wireless broadband communication systems. This is due to its superior performance over other modulation schemes in multi-path environments such as indoor wireless networks [80]. It is currently used in standards such as IEEE 802.11a/g wireless local area network(WLAN), IEEE 802.16, digital audio broadcast (DAB) and high performance radio LAN (HIPERLAN). It is also used in wired communication standards such as asymmetric digital subscriber loop (ADSL). OFDM is also being considered for ultra-wide band (UWB) communication standards [73]-[79]and future 4^{th} generation cellular systems in combination with code division multiple access (CDMA). Ultra-wide band (UWB) has emerged as a popular standard of choice for short-range, high data rate

communication (for wireless personal area network (WPAN) environments), replacing existing standards such as Bluetooth.

UWB devices operate from 3.1GHz to 10.6GHz, with a maximum transmitted power spectral density (PSD) of –41.3dBm/MHz based on federal communications commission (FCC) specification. To enable operation over this wide range of frequencies, UWB is proposed as an overlay technology, i.e. it can coexist with other standards by sharing the spectrum. UWB uses two transmission modes, a carrier-based mode using OFDM modulation [79] and pulse-based mode [75]. While the pulse-based mode uses the entire spectrum available to UWB for transmission, the OFDM-based approach known as MB-OFDM divides the frequency range into multiple bands. The popularity of these wireless devices has led to a proliferation of products in the market that cater to a wide variety of applications. It has also increased the pressure on semiconductor manufacturers to reduce the production costs to ensure success in the market place in the face of stiff competition. To reduce production test costs, novel test techniques are proposed in this work that not only reduce the test time, but also allows the use of low-cost test instrumentation.

2.1 LOW COST EVM TESTING

Measuring the EVM of a system in lieu of individual RF and baseband circuit specifications reduces test time and test cost. Recent advances in ATE instrumentation design such as the incorporation of parallel wideband receivers in the test system, distributed DSP processing, and advanced software allow fast testing of wireless devices. In spite of these advances, EVM testing remains expensive for the manufacturer due to the high costs incurred on the ATE. EVM measurement of wireless devices requires an

ATE that supports precision digital modulation capability. In production testing, this requirement on the RF signal generator translates to higher cost of test instrumentation and higher test cost per device. Also, EVM testing must be performed over a large number of transmitted symbols for high test repeatability. Due to this requirement, current test procedures EVM are time consuming, and therefore, expensive.

The conventional test setup for measuring the EVM of DUT is shown in Figure 6. If the DUT is an RF device like the power amplifier (PA) (DUT 1 in the figure), the measurement setup would require an ATE that has a RF signal source supporting digital modulation and an internal down-conversion receiver for demodulation, and tester DSP for performing the calculations. If the DUT is an integrated receiver chip (DUT 2) with baseband processing capability, the requirements on the ATE are more relaxed. For EVM testing of the transmitter, a receiver in the ATE is used, whereas, for testing an integrated receiver such as a WLAN chipset, the test setup only requires a high-performance signal source supporting digital modulation.

EVM measurements are also used to characterize noisy channels. The test setup and the requirements on the ATE, therefore, change depending on the DUT. However in all cases, the test setup incurs high costs for the manufacturer, primarily due to the high-performance modulation-capable signal sources and receivers. A test scheme that relaxes the requirements on the ATE signal source is required. A novel test methodology for OFDM-based transceivers is presented in this work that relaxes the requirement of high-cost test instrumentation. The proposed approach uses multi-tone signals as test stimuli instead of an OFDM signal, thus reducing the test stimulus generation cost. At the same time, significant test time speedup is obtained.

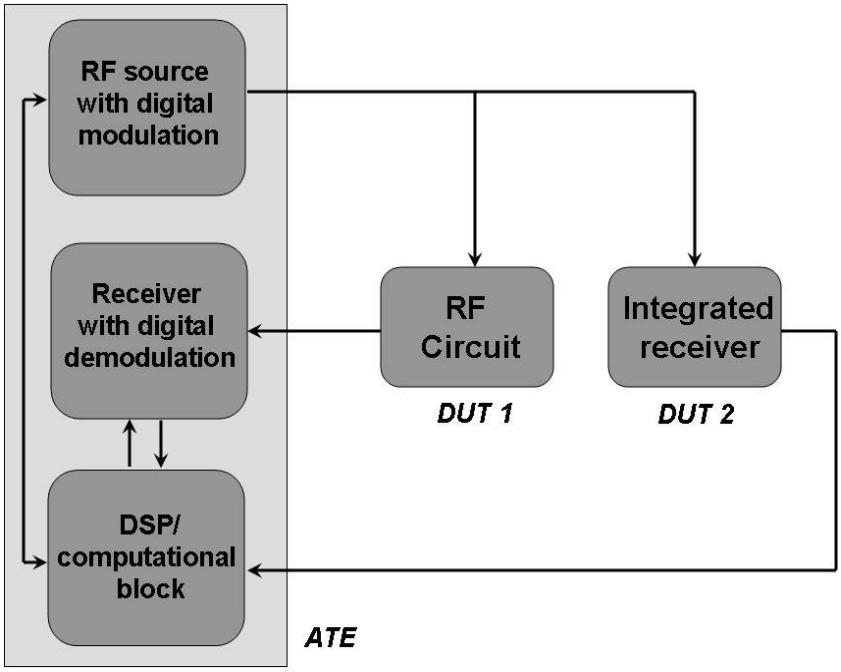


Figure 6 Conventional test setup for measuring EVM.

2.1.1 OFDM Baseband Architecture

In OFDM, the communication channel is divided into a number of equally spaced frequency bands. A subcarrier carrying a portion of the data is then transmitted in each band. Each subcarrier is orthogonal with every other subcarrier in the channel. Thus the subcarriers have a spectral null at all other subcarrier peak values, making the individual carrier frequencies independent of each other. In traditional frequency division multiplexing (FDM) systems, the spacing between the carriers is set to be more than the encoded data rate to avoid overlap and leakage of data to the neighboring bands. This causes an inefficient usage of the spectrum, and results in lower data rates than what can be extracted out of the channel. On the other hand in OFDM, the individual carrier frequencies can be brought closer to each other as the overlap of their spectrums can be

tolerated. Thus, more carriers are squeezed into a given channel bandwidth, thereby increasing the efficiency. The orthogonality property of OFDM, together with the use of a small amount of guard time during data transmission makes the communication robust to multi-path effects. Moreover, in case of narrow-band interference, the affected carriers are turned off selectively, thus making it insensitive to external interference.

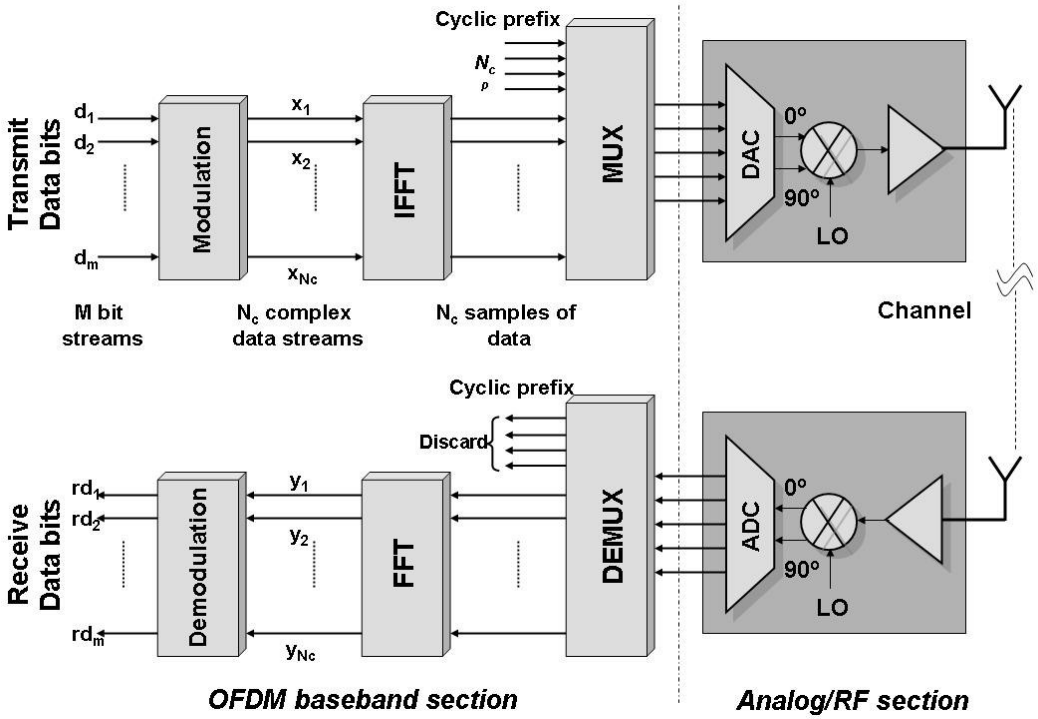


Figure 7 OFDM transmit-receive chain.

Information is modulated onto a carrier by adjusting the carrier's phase, amplitude, or both. An OFDM transmit-receive chain is illustrated in Figure 7. The transmitter takes an input data stream and splits it into N_c parallel data streams, where N_c is the number of carriers. Each of these data streams has a rate that is $1/N_c$ times the original data rate. They are then mapped to N_c different carrier frequencies and combined together using the inverse fast fourier transform (IFFT) to yield a time-domain

waveform. A guard time (T_{cp}), called a cyclic prefix (CP), is added to the waveform to form a symbol. The addition of the guard band prevents the loss of orthogonality between carriers in a multi-path environment. The transmitted waveform is composed of a set of symbols. At the receiver, the received data is cleaved off the guard band and the fast fourier transform (FFT) is performed to yield a set of complex numbers. This complex data set is then demodulated to give the data bits that are then passed further down the chain for baseband processing. Careful selection of system parameters such as the number of carriers and carrier spacing is necessary to reduce inter-symbol interference (ISI). To maintain orthogonality between carriers, it is necessary to ensure that the time period of each block (IFFT output) of the transmitted signal contains one or multiple cycles of each individual sinusoidal carrier. Hence, the system is constructed such that the individual carrier frequencies are an integer multiple of the symbol period *T*. The carrier spacing (Δf) is therefore chosen as

$$\Delta f = \frac{1}{T} \tag{3}$$

2.1.2 Proposed Methodology

To alleviate the requirements of a high performance signal source in the tester, the use of a low-cost multi-tone signal generator is proposed for EVM testing. Multi-tone signal sources are easy to construct and are relatively less expensive compared to other sources with modulation capabilities. Multi-tones can be used to test the performance of the OFDM device for both constant-modulus and variable-modulus modulation schemes. Modulation schemes like quadrature phase shift keying (QPSK), where are all possible constellation points have the same magnitude are known as

constant-modulus, while schemes like quadrature amplitude modulation (16-, 32-, 64-QAM) that have constellation points with more than one magnitude value are referred to as varying-modulus. The QPSK and 16-QAM constellation diagrams are shown in

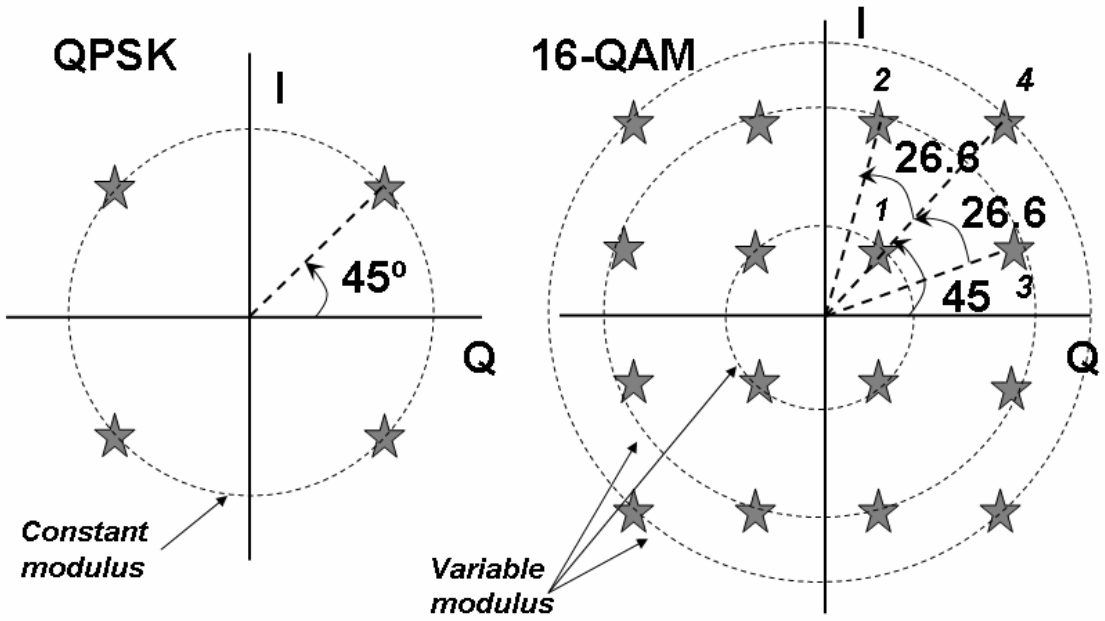


Figure 8 QPSK and 16-QAM constellations

2.1.2.1 Multi-tone Generation for Testing QPSK Modulation

In coherent sampling technique, the sampling of a periodic sine wave is such that an integer number of cycles fit into the pre-defined sampling window. Thus, the relationship between the frequency (f) of the periodic signal and the corresponding sampling frequency (f_{sample}) assuming coherent sampling is given by (3), where N_p and N are positive integers, relatively prime to each other.

$$f = \frac{N_p \times f_{sample}}{N}, N_p, n \in +\mathrm{I}, N = 2^m, \frac{N_p}{N} < \frac{1}{2} \qquad (4)$$

A coherently sampled sine wave ($x_1(n)$) of frequency f and an arbitrary phase shift (θ) can be denoted as

$$x_1(n) = \sin\left(\frac{2\pi f_{sample}\, n}{N} + \theta\right) \qquad (5)$$

Here, the subscript 1 is utilized to denote that $x_1(n)$ is a sine wave of fundamental frequency f., n is an integer multiple of sample period ($T_{sample} = 1/f_{sample}$).

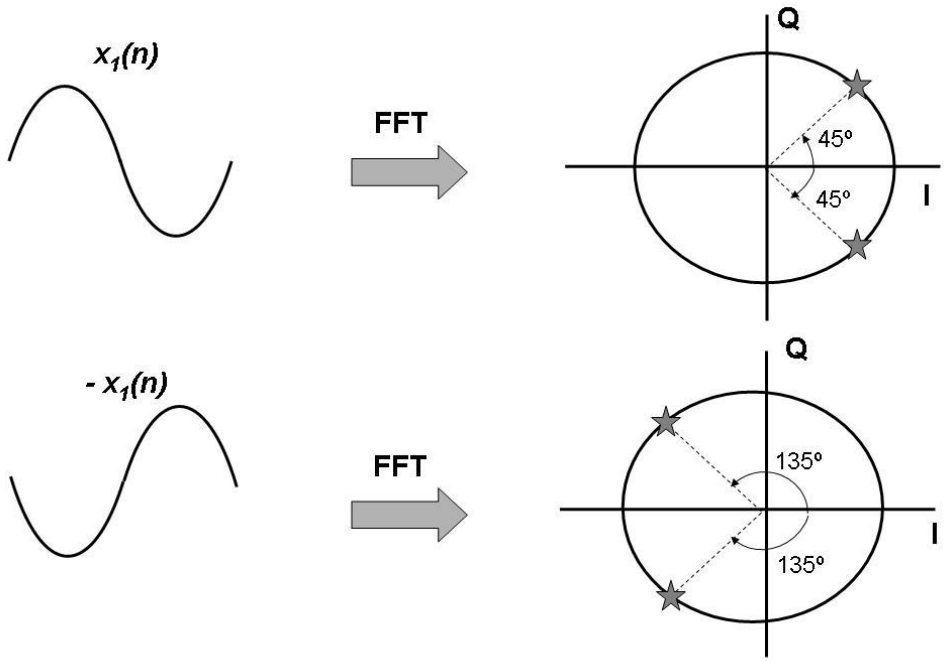


Figure 9 FFT of $x_1(n)$ and $-x_1(n)$ with phase defined by Equation(7).

Performing FFT on $x_1(n)$ gives the following:

$$X_1(k) = \sum_{n=1}^{N} x_1(n) e^{-j2\pi k(n-1)/N} \qquad (6)$$

for k=1,2,..N. Thus, FFT of an N-point waveform $x_1(n)$ generates a set of N complex numbers given by $X_1(k)$. $X_1(k)$ has only two non-zero components of equal magnitude. In other words,

$$X_1(k) = 0, \quad k \neq 2, N \qquad (7)$$

This is because the signal $x_1(n)$ consists of only one frequency component. The non-zero components of $X_1(k)$ appear as constellation points in the complex I/Q plane. For a constellation point to lie on the ±45º line, the magnitudes of the real and imaginary parts should be equal. The constellation points can be forced to appear at 45º and -45º in the complex plane if phase of the sine wave is set as

$$\theta = \left(\frac{\pi}{2} + \frac{\pi}{8} + \cdots \frac{2\pi}{N} \right) \quad [\text{from (3), } N = 2^m] \tag{8}$$

Equation (8) is therefore obtained by equating the real and imaginary parts of $X_1(k)$ in Equation (6). Inverting the waveform $x_1(n)$ and taking the FFT produces constellation points at 135º and -135º degrees in the complex plane. This is equivalent to adding a phase of 180º to $x_1(n)$ as illustrated in Figure 9. Let the p^{th} order harmonic of the fundamental frequency signal $x_1(n)$ be denoted as $x_p(n)$ and be given by,

$$x_p(n) = \sin\left(\frac{2\pi p f_{sample}\, n}{N} + \theta \right) \tag{9}$$

Taking the FFT of the signal $x_p(n)$ produces only two non-zero components of $X_p(k)$ as $x_p(k)$ contains only one frequency component. The non-zero values of $X_p(k)$ result for $k = p+1,\ N-p+1$, which appear as two constellation points in the complex plane.

Next, a two-tone signal $x(n)$ comprising two frequency components ($x_1(n)$ & $x_p(n)$) is considered

$$x(n) = x_1(n) + x_p(n) \tag{10}$$

It is observed that the FFT of this signal produces four non-zero components (constellation points). This is consistent with the earlier discussion that each of the two

frequency components (*f* & *pf*) generate two non-zero components in the fourier transform *X(k)*. The complex I/Q plane therefore contains four constellation points as illustrated in Figure 10. In general, it is to be noted that the FFT of a multi-tone signal produces multiple constellation points at different locations depending on the relation between the sinusoids. By specifically adjusting the phase offsets [81] of each of the individual sinusoids, all the constellation points can be made to appear at the 45º and -45º locations in the I/Q plane. The required phase offsets for a particular frequency are derived here as follows.

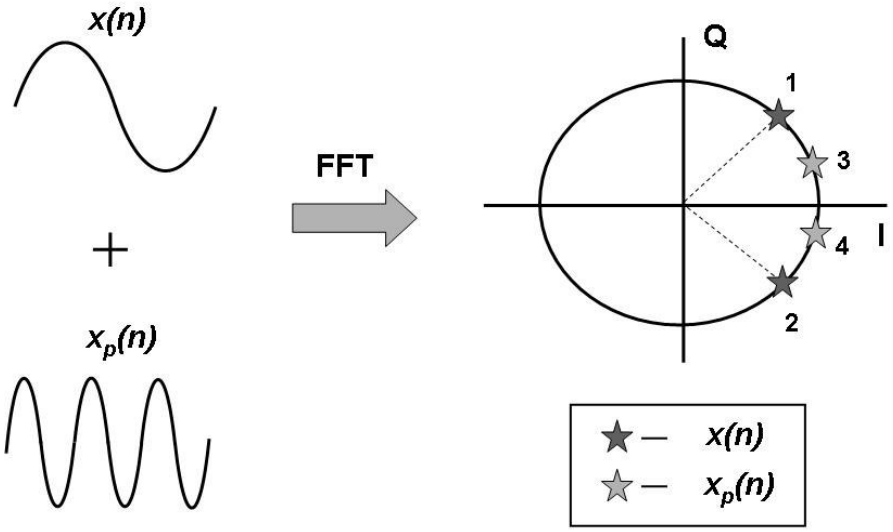


Figure 10 Relation between frequency of the sinusoid and the location of constellation points in I/Q plane.

In Figure 10, constellation points **1** and **2** are contributions of $x_1(n)$ corresponding to the values of $X_1(2)$ and $X_1(N)$ in the computed FFT. Similarly, constellation points **3** and **4** in turn represent $X_p(p+1)$ and $X_p(N-p+1)$ obtained from the FFT of $x_p(n)$. Adding a phase offset to $x_p(n)$ moves the points **3** and **4** around in the unit circle for different phase values, and for a particular phase offset φ_p of $x_p(n)$, these points coincide with **1** and **2**. In

general, a multi-tone signal with constellation points at only the ±45º locations can be generated by adding specific phase offsets to each of the multi-tone components. This idea is illustrated in Figure 11.

From Equation (4), it is evident that a time window of N sample points contains N_p cycles of signal $x_1(n)$. The corresponding time window also captures $p \times N_p$ cycles of the p^{th} harmonic signal $x_p(n)$.Let the phase shifted version of $x_p(n)$ be denoted as $x_p'(n)$, and the corresponding Fourier domain signal be $X_p'(k)$. From Fourier theory,

$$X_p'(k) = X_p(k)e^{-j\varphi_p} \qquad (11)$$

For the constellation points **3** and **4** to coincide with **1** and **2**, respectively, their magnitudes should be equal. Therefore

$$X_p'(p+1) = X_1(2) \qquad (12)$$

The derivation of the required phase shift φ_p is shown by solving Equation (12).

Before solving the above equation, basic relations between the signals of different frequencies are derived. Consider an N-point time window that contains the fundamental and higher harmonic signal waveforms as shown in Figure 12. The figure plots sinusoids of fundamental frequency (f) and the 2nd and 3rd order harmonics with a window size of 16 samples ($N=16$). From Figure 12, a simple relationship between the magnitudes of sample points on the different waveforms is observed. For example, $x_3(1)$ is equal in value to $x_1(3)$, and $x_2(5)$ is equal in value to $x_1(10)$. In general, it is noted that the value of the n^{th} time point in the p^{th} harmonic signal ($x_p(n)$) is equivalent in magnitude to the $p \times n$ time point of the fundamental signal ($x_1(pn)$) for any value of p and n. Thus, for any combination of p and n, we have $x_p(n) = x_1(pn)$. Rewriting this relation, we have

$$x_p(n) = x_1(pn) = x_1(n - n(1-p)) \qquad (13)$$

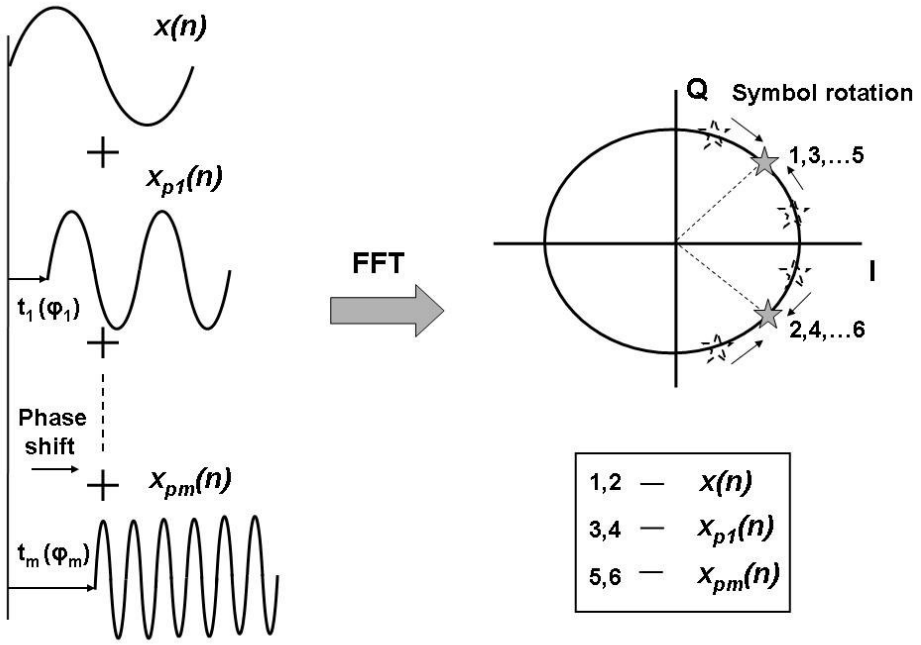


Figure 11 Adding multiple phase-shifted multi-tones to produce constellation points at the desired ±45º locations in the I/Q plane

Equation (13) states that $x_p(n)$ is equivalent in value to a sample point on the fundamental frequency sinusoid that is time-shifted by $n(1-p)$ sample points from index n. This shift in time domain translates to phase shift of $e^{-j2\pi n(1-p)/N}$ in the frequency domain.

With this knowledge, Equation (12) is solved for the phase shift φ_p as follows. Using the definitions given in Equations (6) and (11), the fourier transform of the phase shifted signal $x_p'(n)$ is written as follows

$$X_p'(p+1) = \sum_{n=1}^{N} (x_p(n) e^{-j2\pi(n-1)(p)/N}) e^{-j\varphi_p} \qquad (14)$$

Substituting for $x_p(n)$ from Equation (13) in Equation (14) gives

$$X'_p(p+1) = \sum_{n=1}^{N} x(n) e^{-j(2\pi(n-p)/N+\varphi)} \tag{15}$$

Using the above relation, Equation (12) is rewritten as

$$\sum_{n=1}^{N} x(n) e^{-j(2\pi(n-p)/N+\varphi)} = \sum_{n=1}^{N} x(n) e^{-j2\pi(n-1)/N} \tag{16}$$

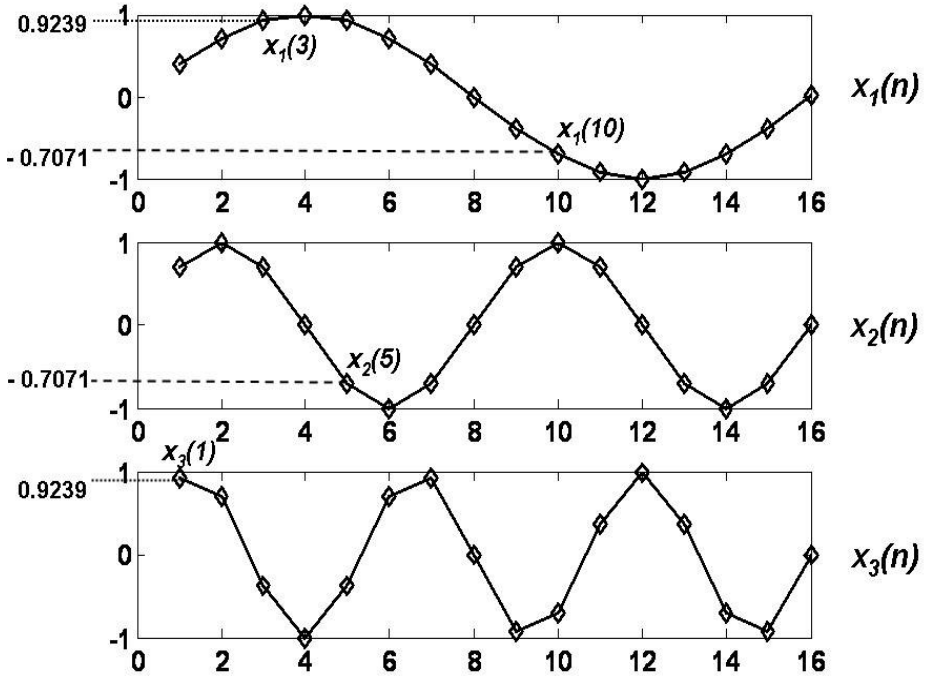


Figure 12 Relation between sample points of different sine waveforms

From the above equation, the phase shift φ_p is obtained as

$$\varphi_p = -\frac{2\pi(1-p)}{N} \tag{17}$$

Thus, by adding a phase shift ($\theta+\varphi_p$) given by Equations (8) and (17) to a sinusoid $x_p(n)$, the corresponding FFT produces constellation points at ±45° locations. The constellation pair at ±135° is in turn obtained by adding an additional phase of 180° to this phase-shifted sinusoid. Thus, a two-tone test signal can be generated with required

phase offsets that produce all the four constellation points corresponding to a QPSK-modulated signal. The magnitude of both the tones is equal as all the four constellation points in QPSK modulation are equidistant from the origin. A WLAN OFDM transmitter modulates data on to 52 active subcarriers as defined in the standard IEEE 802.11g. From the above discussed approach, a multi-tone test signal (up to 52 tones) that mimics a QPSK-modulated OFDM signal can be used to test an OFDM receiver. The multi-tone test signal can be generated using a low-cost signal source with limited programming capability.

2.1.2.2 Multi-tone Generation for Higher Modulations

In 16-QAM modulation, all the constellation points are not of the same magnitude. The constellation plot for a 16-QAM signal was shown in Figure 8. Test signal generation in this case requires some additional consideration. A minimum of eight different tones is required to generate all the required 16 points of 16-QAM constellation as each frequency produces two constellation points. The trick here is to ensure that constellation points appear at the right locations. While the magnitude of sinusoids used to generate QPSK were all equal, three different magnitudes are required to generate the 16-QAM constellation. This is understood through a closer inspection of one of the quadrants of the 16-QAM constellation. For example, let us consider the first quadrant of I-Q plane in. It consists of four constellation points that represent three different magnitudes and phases between them. The constellation points **2** and **3** have the same magnitude whereas the points **1** and **4** have two different magnitudes. The relation between the magnitudes of these four constellation points is obtained through simple geometrical calculations

$$mag(4) = \frac{3}{\sqrt{5}} mag(2,3) = 3mag(1) \qquad (18)$$

The phase of constellation points **1** and **4** is 45º, which is obtained by adding phase offsets equal to $\theta+\varphi_p$ as explained earlier. But phases of points **2** and **3** are about ±26.6º away from the 45º line. These points can therefore be generated by first forcing them on to the 45º using a phase offset of $\theta+\varphi_p$, and then adding an additional ±26.6º. The constellation points in the other quadrants can similarly be obtained.

A summary of the magnitude and phase values required for the eight different frequencies in the multi-tone waveform needed to generate the 16-QAM constellation is given in TABLE . For example, the sinusoid at frequency *3f* generates the constellation point **2** and its corresponding mirror image in the fourth quadrant. The required phase offset for generating these points using a sinusoid of frequency *3f* is $\theta+\varphi_3+26.6$. The first four frequencies (*f* to *4f*) in TABLE I are used to generate all the constellation points in the 1st and 4th quadrants, while the next four frequencies (*5f* to *8f*) generate the constellation points in the 2nd and 3rd quadrants. Additional tones when added to these eight sinusoids can generate additional symbols at each of these 16 constellation points. Moreover, random transitions between these constellation points can be introduced by shuffling the tones and their phases at random. Thus, a multi-tone test stimulus for WLAN OFDM systems can be generated by adding 52 different tones with respective magnitudes and phases such that a constellation corresponding to any desired modulation scheme. Common modulation schemes include binary phase shift keying (BPSK), QPSK, 16-, 32-, 64-QAM etc. Test generation for 32- and 64-QAM follows an extension of the approach described for 16-QAM.

TABLE 1 Multi-tone generation for 16-QAM: magnitudes and phases of individual tones

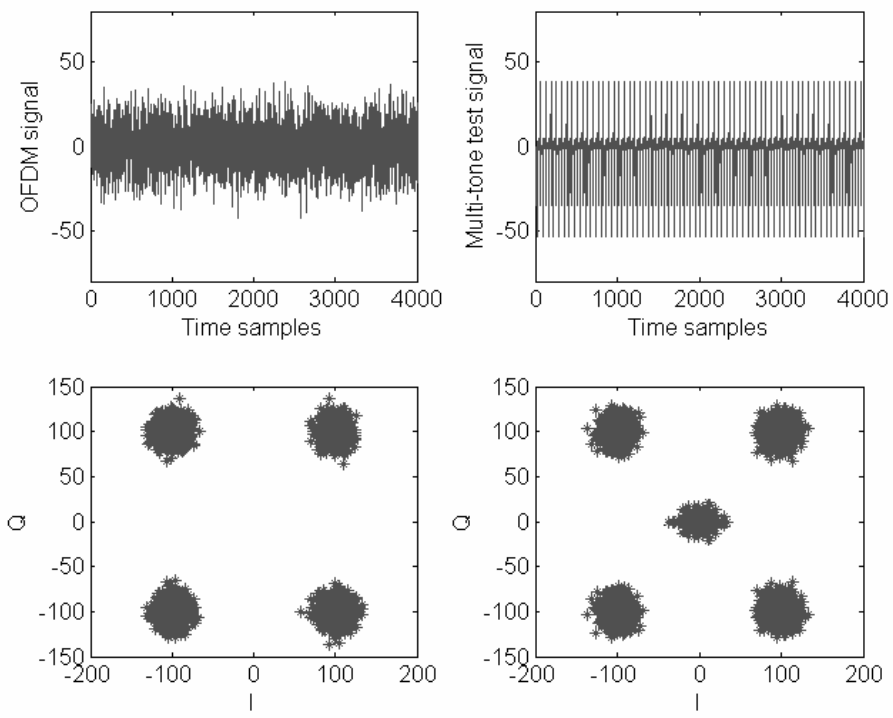
Frequency	Magnitude	Phase
f	1	θ
2f	$\sqrt{5}$	$\theta + \varphi_2$ -26.6
3f	$\sqrt{5}$	$\theta + \varphi_3$ +26.6
4f	3	$\theta + \varphi_4$
5f	1	$\theta + \varphi_5$+ 180
6f	$\sqrt{5}$	$\theta + \varphi_6$ + 153.4
7f	$\sqrt{5}$	$\theta + \varphi_7$ + 206.6
8f	3	$\theta + \varphi_8$+180

2.1.3 Evaluation of the Proposed Approach for EVM Test

In order to study the feasibility of using multi-tones for EVM testing of OFDM devices, MATLAB simulations for standard test and proposed test are performed on a IEEE 802.11g OFDM transceiver module. In the transmission chain, random data bits obtained from a noise generator are used to generate a baseband OFDM signal with QPSK/16, 64-QAM modulations, respectively. The transmission chain generates an actual OFDM test signal. This signal is then looped back into the receive chain, where it is demodulated and the symbols are decoded. A sufficiently large number of symbols (~10,000) are transmitted to calculate the EVM of the receiver. Next, a multi-tone test stimulus (proposed approach) that generates the exact constellation as the OFDM

modulation is generated and looped back into the receiver, where the EVM is again calculated from the decoded symbols. An equal number of symbols are transmitted in both cases to evaluate the accuracy of the proposed approach. A normally distributed random noise is added in the channel to provide variations in the received signal and modify the SNR.

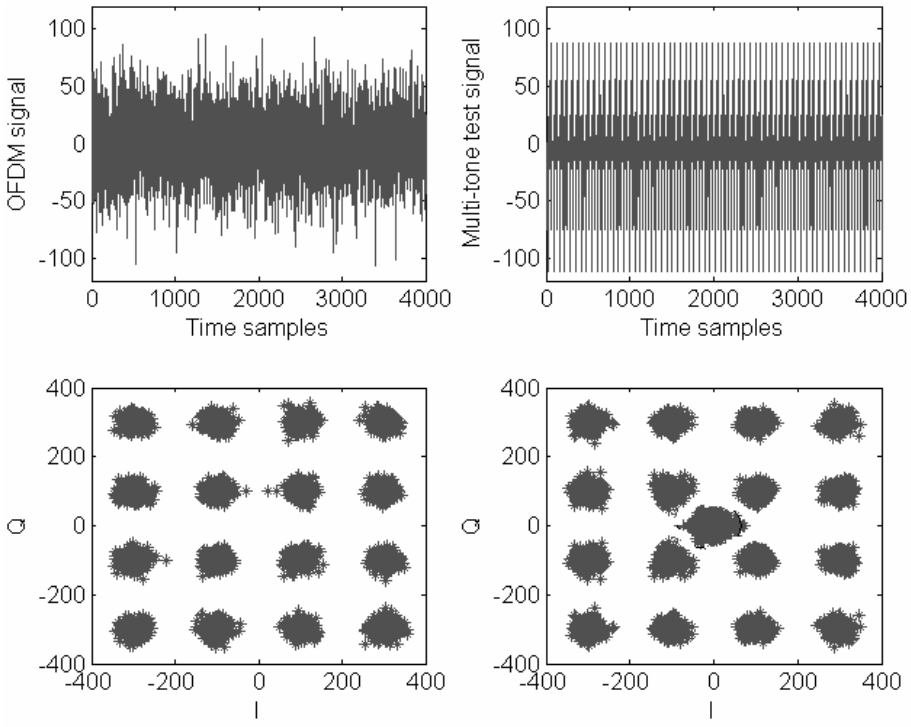
Figure 13 shows the transmitted QPSK-modulated OFDM signal and the corresponding multi-tone signal (test stimuli) used for testing the transceiver chain. The decoded constellations from the two signals, respectively, are shown in the plots below. In the proposed approach, some symbols that fall at the origin apart from the four locations corresponding to QPSK modulation. These occur due to the null carriers in the test stimulus. The signal and constellation plots for 16-QAM modulation are shown in Figure 14. The spread of symbols and the corresponding EVM value is dependent on the fidelity of the received signal. The plots of computed EVM for QPSK and 16-QAM modulations for varying noise levels (hence SNR) are shown in Figure 15. In this case, the EVM calculated from the multi-tone test waveform closely tracks the EVM obtained for the OFDM system for both QPSK and 16-QAM modulations. The error is less than 3% for the range of SNR and EVM values shown in the plot.



(a) (b)

Figure 13 Transmitted signal and decoded symbols for QPSK modulation. (a) OFDM signal (b) Proposed multi-tone signal

In a real communication system, the received signal quality is dependent not only on the noise in the channel and device but also the non-idealities such as non-linearity, phase noise, gain/phase mismatch etc. present in the system. In the presence of these non-idealities, it is observed that the relationship between the EVM values obtained from the proposed and standard approaches is not straightforward. Due to the complexity of the problem, a multi-parameter correlation-based approach is necessary to build a relationship between the two EVM values. In the following discussion, the procedure for accurately estimating EVM using the multi-tone test stimulus is provided followed by a comparison with the computed EVM from standard test.



(a) (b)

Figure 14 Transmitted signal and decoded symbols for 16-QAM modulation. (a) OFDM signal (b) Proposed multi-tone signal

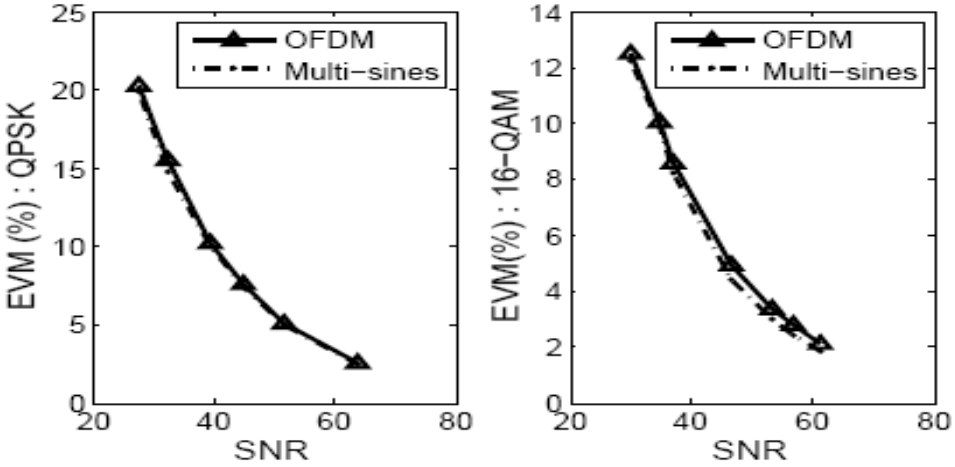


Figure 15 EVM values for various signal fidelity levels: Effect of noise addition in the channel

'*Alternate*' test techniques have been proposed in the literature to estimate circuit and system specifications from specific features captured from a test response. These techniques use correlation-based regression models such as multivariate adaptive regression splines (MARS) to accurately predict specifications of interest. In this work, MARS models are trained and then used to estimate the EVM from specific constellation features obtained from the proposed test. It is assumed that a defect filter is used to screen out defective parts before applying the alternate test technique. The approach is illustrated in Figure 16. To develop (train) MARS models, a set of receiver instances are first generated by randomly perturbing the behavioral parameters corresponding to gain, non-linearity, phase noise etc. Standard OFDM test and multi-tone test is performed on these devices, and the test results are used for training the MARS model as shown in the Figure 16. Contributions to EVM, i.e. scattering of symbols around ideal constellation points come from the following sources

- The inherent noise in the DUT and measurement setup: This causes the symbols to scatter evenly around the ideal constellation points. This effect was observed in decoded constellations of Figure 13 and Figure 14.
- Non-idealities in the system such as non-linearity, gain/phase mismatch in the quadrature modulator/demodulator, and phase noise etc.: These effects cause the entire constellation cloud to shift from the ideal location in a certain direction.

The relative dependence of EVM on these two factors depends on the signal fidelity levels. For example, for a signal with high SNR, the effects of non-idealities dominate EVM computation. For low SNR signals, the noise contribution is more dominant. In either case, if the contributions of noise and system non-idealities can be

quantified, this information can be used to accurately estimate EVM. From the constellation plot obtained for multi-tone test stimulus, required features such as noise level (*No*) and constellation displacement vectors ($V\vec{1}, V\vec{2}, V\vec{3}, V\vec{4}$) are extracted and fed as input to MARS. The displacement vectors are calculated as the error vectors between the center of mass of the constellation cloud and their corresponding ideal locations. Since the symbols that appear at the origin of the output plot are due to the null carriers (zero magnitude), the scatter is primarily due to the noise in the system and test setup. The noise contribution (*No*) is extracted by computing the sum of the magnitudes of the symbols that fall at the center of the constellation plot. During pre-production characterization of the device, the MARS model is trained to estimate the actual EVM (obtained from standard test) from a set of input parameters (*I* in Figure 16) obtained from multi-tone test. The training is usually done for a set of *l* training instances. During actual production test, the trained MARS model is then used to estimate EVM for different DUTs.

Simulations are performed to prove the feasibility of the approach. A set of 200 receiver instances are generated by perturbing the following behavioral parameters in the model – system gain, non-linearity in the RF front-end, magnitude and phase mismatch between the I and Q paths, oscillator phase noise and system noise figure. Among these, 160 instances (here $l = 160$) are used for training the MARS model. The remaining 40 instances are used for validating the accuracy of the MARS model. To do this, standard OFDM test and the proposed test along with MARS prediction are performed on these 40 receiver instances. The results of simulation are plotted in Figure 17. The estimated

EVM values closely track the 45º line proving that they are calculated with good accuracy. The relative error is less than 3%.

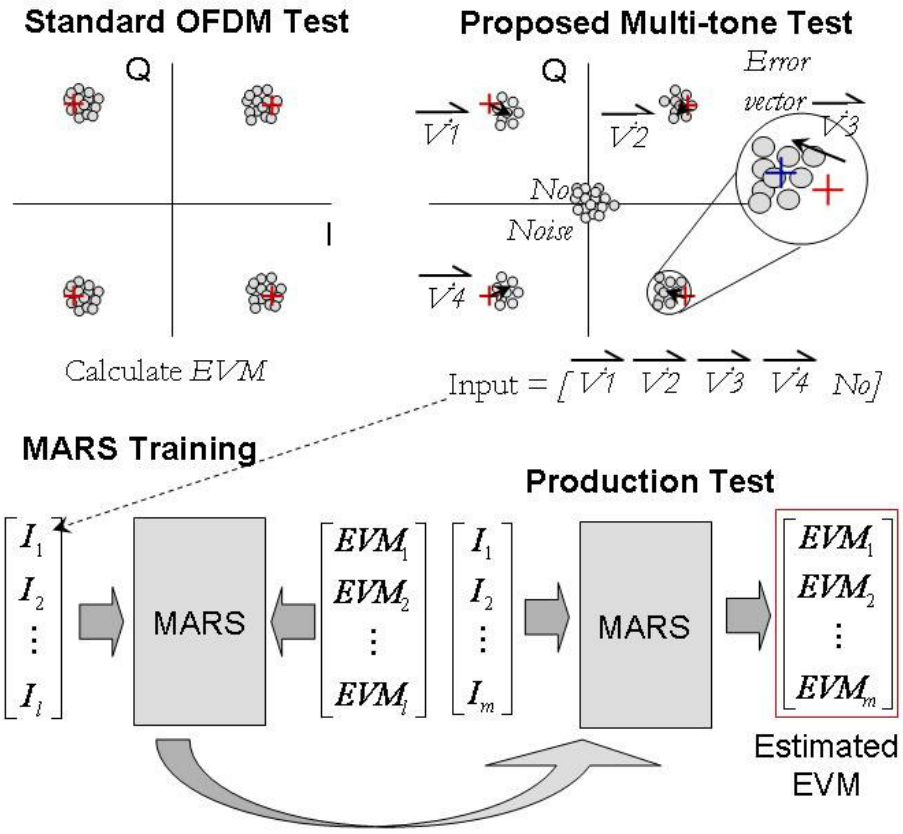


Figure 16 Proposed test approach for EVM

Next, a field programmable gate array (FPGA)-based hardware test setup is used to verify the proposed theory using measurements. A baseband OFDM transceiver was implemented in hardware using an Altera Stratix-II development kit [81]. The system is designed in Simulink/Matlab [82] using custom blocks provided by Altera. The hardware realization of the design was then created on the Stratix II FPGA chip in the development board. The Stratix development board also consists of high-speed ADC and DAC converters that permit external loopback functionalities through analog/RF blocks. The DAC is of 14-bit precision while the ADC has a 12-bit precision.

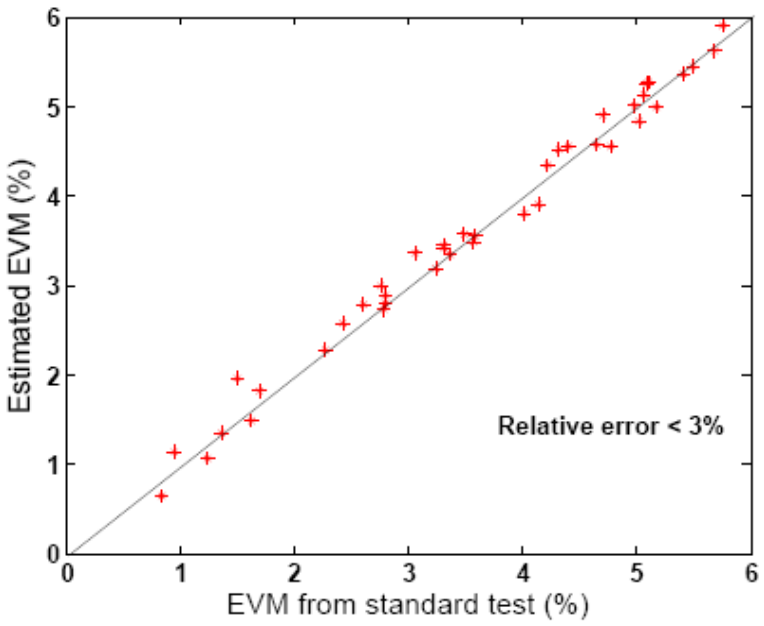


Figure 17 Estimated EVM from proposed test vs. actual EVM from standard test

The hardware implementation of the baseband transmit-receive chains of the OFDM transceiver are used to study the performance of the system. The top-level schematic of the system containing the DAC and ADC is shown in Figure 18. A direct external loopback of the transmitted baseband OFDM signal is done to test the proper functioning of the baseband receiver. The FPGA device is operated at a clock frequency of 25 MHz which sets the bandwidth of the baseband signal. Thus, the fundamental time period of the OFDM signal is 40nsec, and the time period of its lowest frequency component is 64 x 40nsec = 2.56us. This specification is identical to the baseband specification of an IEEE 802.11a/g device. Figure 19 shows a transmitted QPSK-modulated OFDM signal and the corresponding loopback received signal. The data is captured by an instance of SignalTap II logic analyzer provided by Altera. As seen from the plot shown in Figure 19, there is a loopback delay (12 clock cycles) between the transmitted and received OFDM signals.

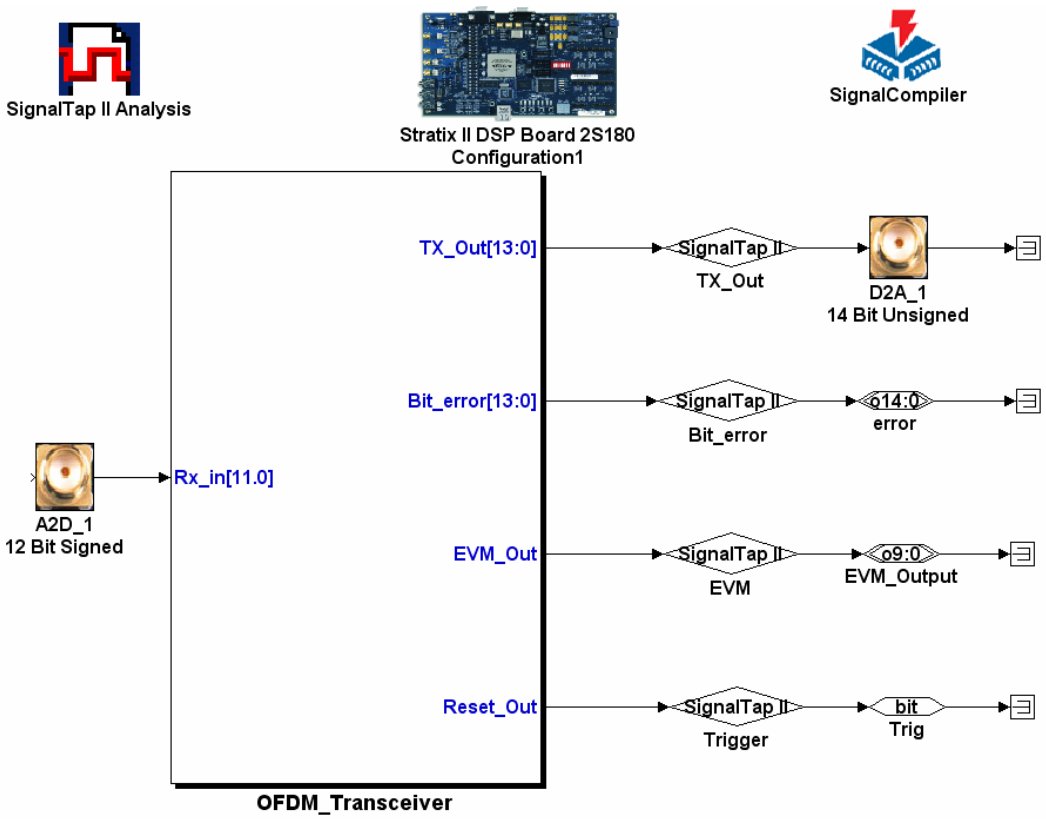


Figure 18 Top-level schematic of the baseband OFDM transceiver

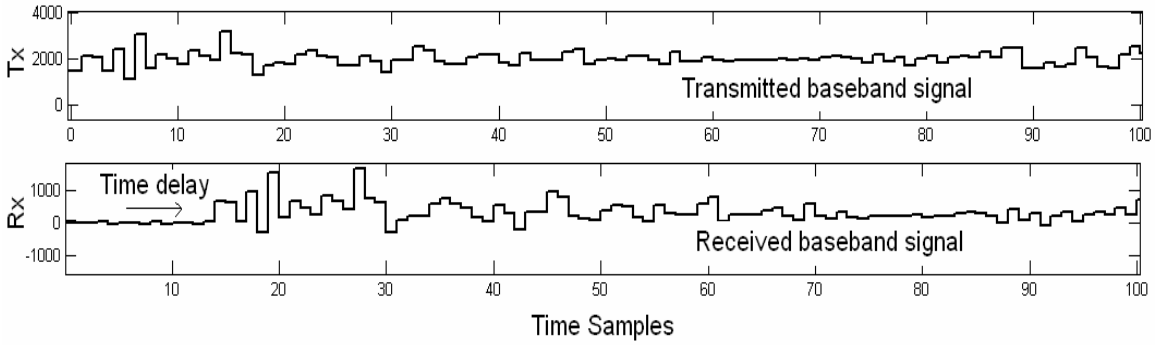


Figure 19 Transmitted and received baseband OFDM signal captured from FPGA board

Next, loopback of the OFDM signal is implemented with the addition of RF front-end section. For this purpose, an RF front-end working at 2.4 GHz is designed using discrete transistors and off-the-shelf components on printed circuit board (PCB). The front-end design uses a super-heterodyne architecture consisting of an up-

conversion mixer and PA in the transmit section and low-noise amplifier (LNA) and down-conversion mixer in the receive section. The second mixing stage that incorporates quadrature modulation (I and Q channels) is implemented digitally in the FPGA. The PA output is looped back to the LNA input through a power-combiner that is fed by a noise generator. The noise generator adds noise to the baseband signal replicating a noisy channel. The RF-front-end and the test-setup is shown in Figure 20.

The delay between the transmitted and loopback data in this case is once again observed to be 13 clock cycles. The captured transmitted and received QPSK-modulated symbol waveforms are shown in Figure 21. The symbols are complex consisting of real and imaginary components. As observed in Figure 21, the received symbols have varying magnitudes and phase (symbol spread) signifying the presence of the non-idealities in the transmit-receive chain that includes the FPGA board, RF section and channel. The addition of noise from the signal generator introduces further variations in the received signal. This causes a spread of the symbol constellation in the complex I-Q plane as seen in the plots. This symbol spread in turn leads to a non-zero EVM value. As the noise contribution to the system increases, so does the computed EVM.

With the above test setup, the sensitivity of the OFDM transceiver to noise is studied. EVM is calculated by comparing the transmitted and received QPSK symbols and processing the cumulative difference in the FPGA. The calculated EVM values for different SNR are given in the second column of Table II. The EVM values are significantly higher than the simulation results mainly due to the non-idealities of the ADC, DAC and the RF section.

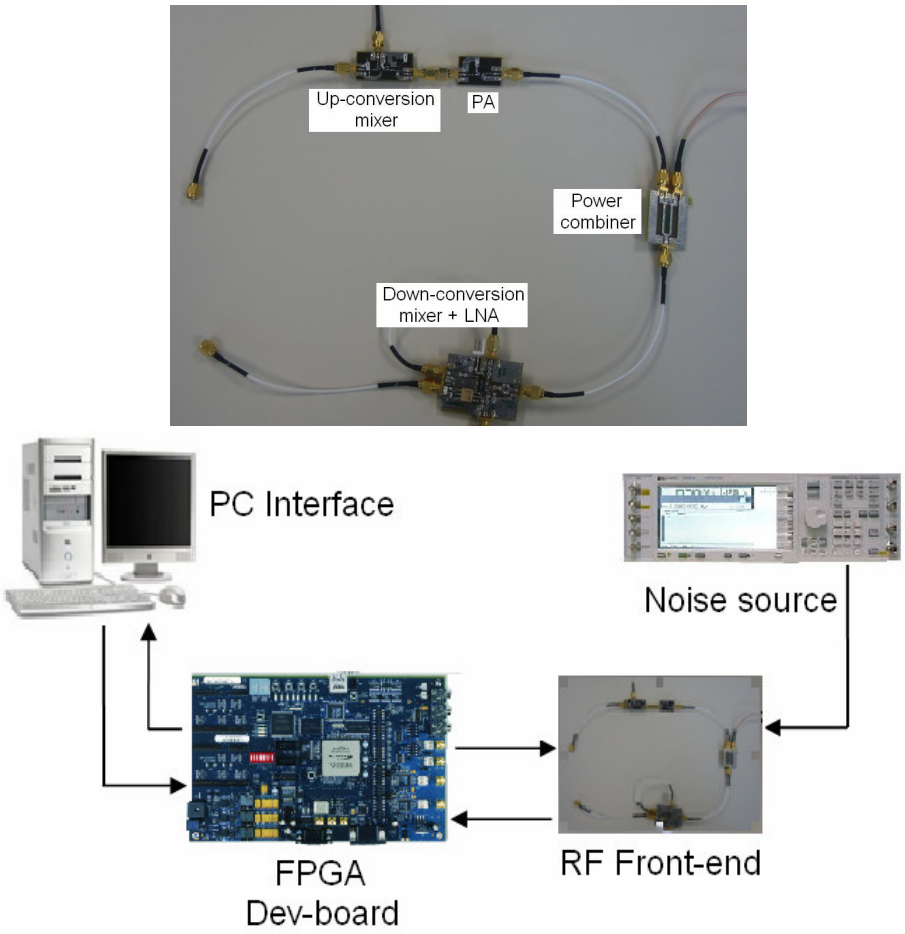


Figure 20 RF front-end and test-setup used for measuring EVM

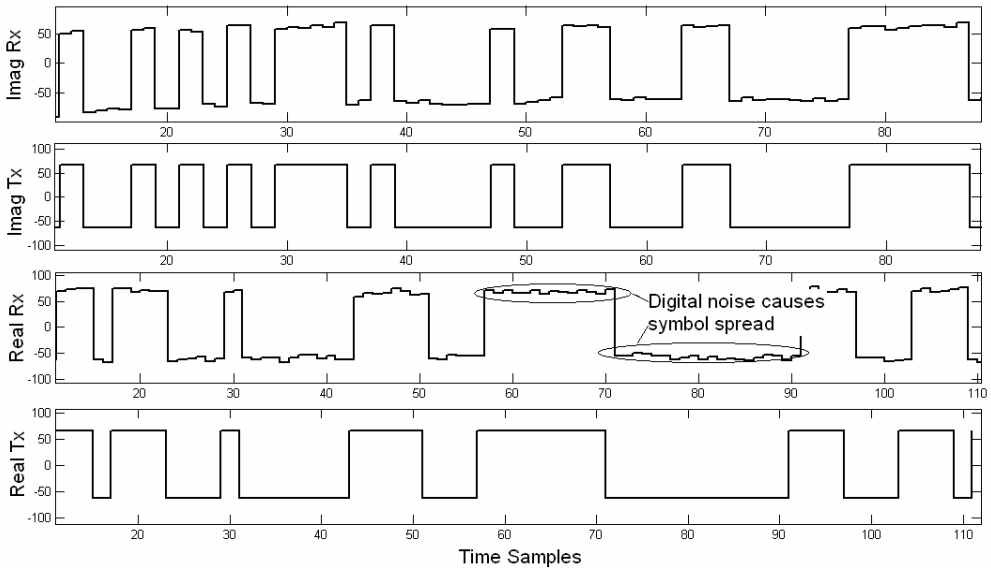


Figure 21 Signal capture of transmitted and received QPSK symbols

TABLE 2 EVM measurements for a QPSK-modulated signal using standard and proposed test approach

SNR	Standard approach EVM (%)	Proposed approach EVM (%)
50 dB	26.9	22.5
40 dB	33.0	28.3
35 dB	42.3	37.1
30 dB	62.3	57.0

EVM of the transceiver is computed using the proposed multi-tone approach. For this purpose, multi-tones are generated using the FPGA and looped back into the receiver through the RF section. The EVM computed using the proposed approach follows a similar trend compared to the standard approach though they are about 5% lower than the values obtained for the OFDM case. This is due to the effect of the ADC-DAC combination of the FPGA development board. Since the ADC precision (12 bits) is 2 bits lower than that of the DAC (14 bits), there is some loss of information in the loopback process. OFDM baseband signal is more sensitive to data loss compared to the multi-sine signal used here, especially for the sample values near zero. During production test, such effects need to be calibrated in advance before employing the proposed approach. But the results obtained from the standard and proposed test approaches follow similar trends. In summary, the proposed approach offers an effective method to test for EVM of DUTs like PA (transmitters) or integrated receivers using low-cost hardware.

2.1.4 Test Stimulus Generation for Phase Noise Estimation

In addition to enabling EVM test using low cost signal sources, a test generation method for accurate prediction of phase noise is proposed. In the proposed approach, data is modulated on to only some of the carriers while leaving a few of the subcarriers empty as illustrated in Figure 22. This is equivalent to adding *N'* multi-tones with adjusted phases, where *N*' is lesser than *N*, the length of IFFT/FFT. This causes some symbols to appear at the origin of the I/Q plane. These constellation points are a manifestation of 'nulls' in the carriers. Each null carrier produces a pair of constellation points at the origin. The purpose of having null carriers is to isolate the effect of noise, thereby, enabling accurate estimation of this specification. This is because null carriers are not significantly affected deterministic effects such as gain variations, non-linearity, I/Q mismatch etc. as no data is modulated on to these carriers. If the device is operated in the linear region, only the cumulative effects of noise contributors such as phase noise, ADC quantization noise, and ADC sampling jitter show up on the null carriers – i.e. symbols that fall at the origin of the I/Q plane. Symbols at other locations other than the ones that fall at the origin are affected by all the impairments present in the system. Moreover, the test stimulus can be specifically designed using phase shifts that produce a low peak-to-average ratio such that the non-linearities of the system are not exercised.

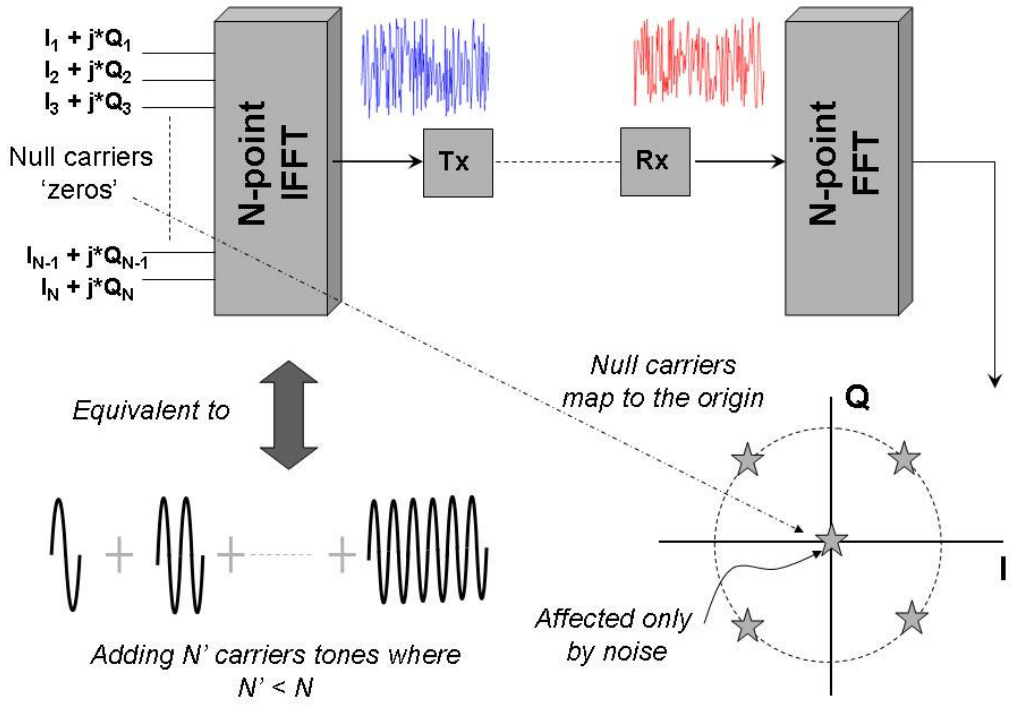


Figure 22 Proposed approach for phase noise estimation

Thus by characterizing the spread about the symbols around the origin, the effect of noise sources can be accurately quantified. Thus, the phase noise specification of the device can be accurately measured assuming its effect is more dominant than the other noise contributing factors. Simulations are performed on an RF front-end to study the proposed approach to test the phase noise and EVM specifications. For this purpose, a multi-tone test stimulus is synthesized first. The number of tones used for the test is N/2, where N is the FFT/IFFT length. The phase shifts of these tones were set such that the obtained constellations correspond to either QPSK or 16-QAM modulations. The remaining N/2 tones are not modulated with any data, and serve as the null carriers. The symbols corresponding to these carriers appear at the origin of the I/Q plane as observed

in Figure 23. The constellation plots obtained when all the tones are used are also plotted in the figure for comparison. As explained earlier, if the device is operated in the linear region the scatter of these symbols is only due to the phase noise and ADC quantization noise (1-least significant bit (LSB) was added).

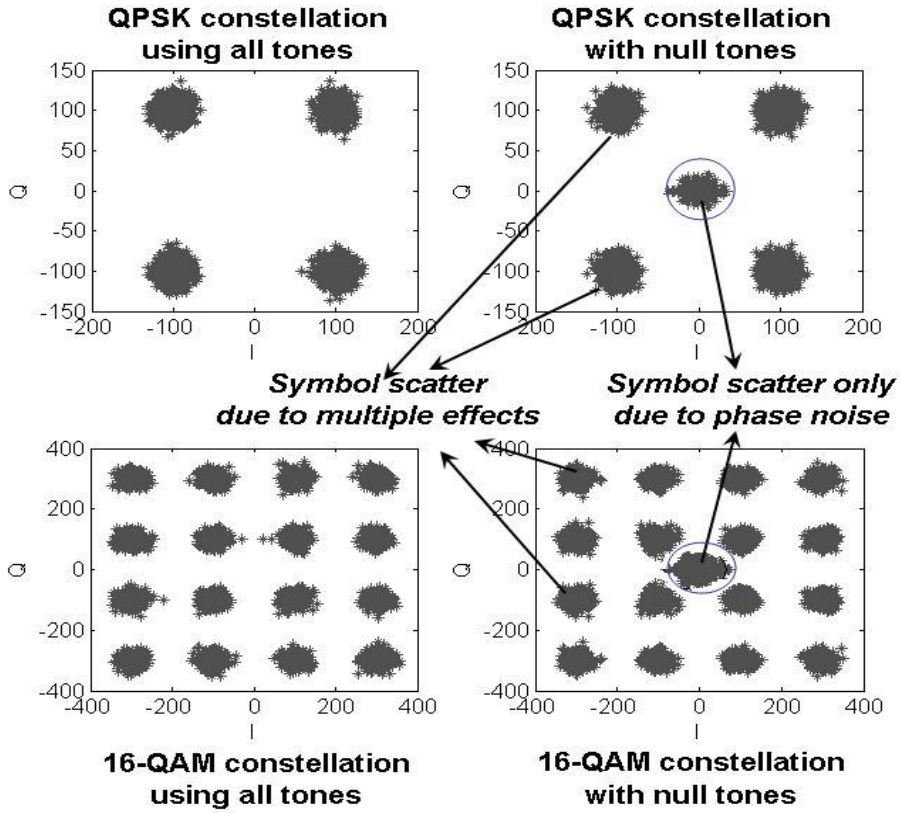


Figure 23 QPSK and 16-QAM constellations for standard and proposed approach

Simulations are performed to estimate the phase noise specification first. The results are plotted for 30 different devices in Figure 24. The 64-QAM constellation plot generated for the test is shown along with the prediction plot for phase noise. Phase noise is computed by calculating the magnitude spread of the symbols that fall at the origin of the constellation plot. The relation between this magnitude spread (*No*) and phase specification is pre-characterized over a set of devices and stored in a look-up-table

(LUT). During the actual test process, the magnitude spread (*No*) is calculated for each device and the phase noise specification is directly extracted from the LUT. Test results show very good estimating accuracy for phase noise (error < 2%). The test can be performed on a transceiver in loopback mode where the on-board DSP is used to compute the phase noise. It should be noted here that the magnitude spread (*No*) is a function of not only the phase noise but also of the other noise contributing factors such as ADC quantization error, sampling jitter etc.

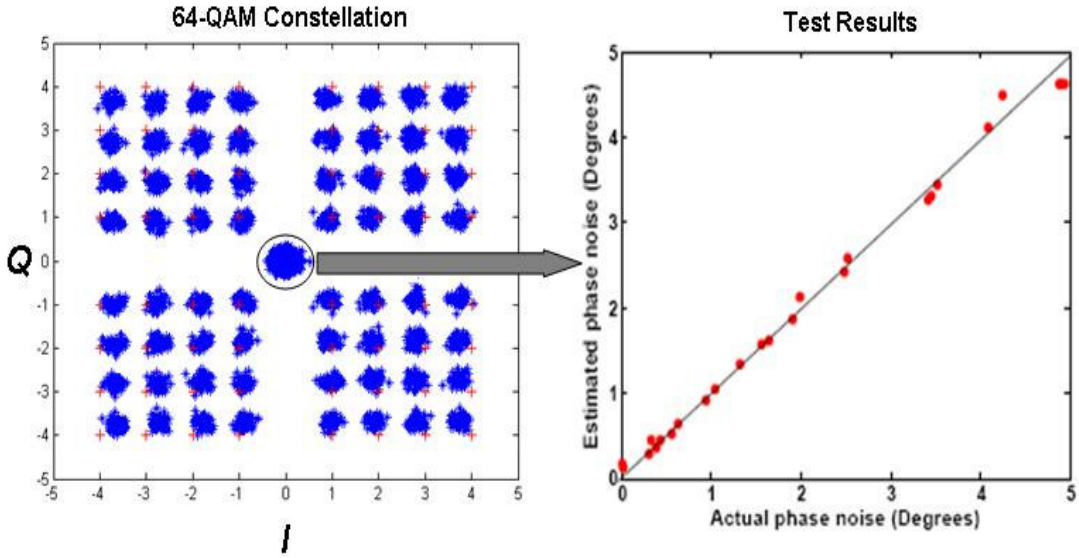


Figure 24 Phase noise estimation from symbols at the origin

2.1.5 Test Time Reduction for EVM

EVM is dependent on several factors including gain variations, non-linearity, I/Q mismatch, and noise effects etc. During the test process, specifications such as gain, IIP3 (non-linearity), I/Q mismatch are usually measured using circuit-level tests. Simulations studies were conducted to ascertain if EVM of the transceiver could be estimated from the measured circuit-level specifications. As observed in the Figure 25 (a), the estimation accuracy (from MARS) is not good if only the above specifications are used for

estimation proving that EVM is strongly dependent on noise contributions as well. Next, EVM estimation is performed by using the noise (*No*) metric as the additional input to MARS *for the same set of devices*.

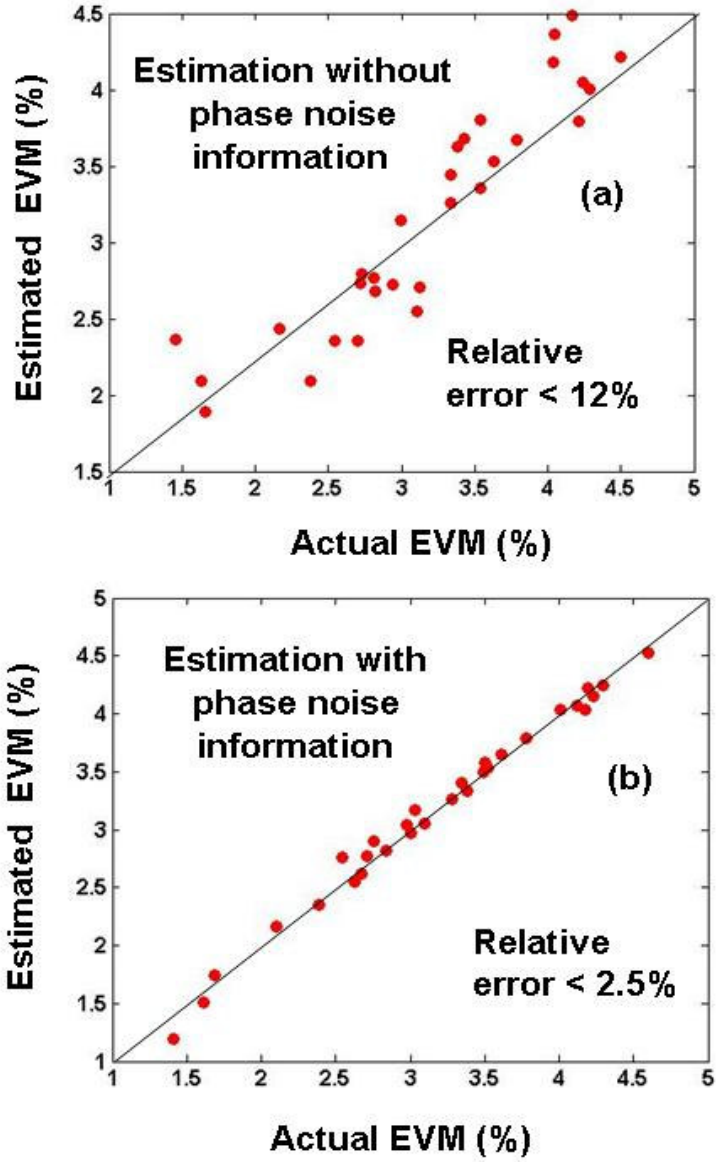


Figure 25 Test time reduction: EVM estimation from circuit-level specifications and noise metric *No*

Computing *No* is very fast requiring only about 3 or 4 frames of OFDM modulated data. Performing a 128-point FFT on modulated data produces an OFDM

frame that produces an equal number (N=128) of symbols in the constellation plot. Among these if 64 are designed to fall on the 64 locations corresponding to a 64-QAM constellation, the remaining 64 can be forced to fall at the origin (null carriers). Thus, processing about 4 frames of 64-QAM modulated OFDM produces 4x64 (= 256) symbols at the origin of the constellation plot. This suffices for accurate noise estimation from the constellation. In the standard approach for EVM testing, a large number of bits need to be transmitted to ensure sufficient number of symbols at all the 64 constellation points, whereas in our approach we need symbols at only one location, the origin. Thus, there is significant test time savings (*64X*). Alternately, a short multi-tone sequence containing null carriers could also be used as the test stimulus instead of an OFDM transmitter. Using the computed *No* in MARS, it is observed in Figure 25 (b) that EVM prediction accuracy is good (relative error< 2.5%). This proves that complex system-level specifications such as EVM can be accurately measured using circuit-level measurements, and simple constellation-based noise estimation procedure as discussed in this work. Employing this approach significantly reduces the test time for EVM.

2.1.6 Advantages of the Proposed Approach

In summary, the advantages of using the proposed test approaches are outlined as follows.

- Using multi-tones for testing OFDM-based receivers is ‘simple’ and can be easily performed using a low-cost multi-tone source with limited programming capability. Alternately, a FPGA chipset may be used to generate the base band multi-tone stimulus and an up-conversion module can be used to shift the signal up to the desired frequency.

- Test stimulus generation in the proposed approach is quite general and platform independent. Test stimulus for several different OFDM-based communication schemes such as WLAN, WiMAX, and ADSL etc. can be easily generated using simple rack-and-stack equipment or low-cost FPGA. To do this, only LUTs containing the frequency indexes and phase shifts for different modulations need to be stored. This significantly reduces the amount of tester memory required.
- Phase noise specification can be tested by using null carriers in test stimulus. The null carriers generate symbols (constellation points) at the origin which are affected predominantly by noise in the system. Thus, quantifying the symbol scatter at the origin enables the accurate prediction of EVM.
- Characterization of phase noise specification along with other impairments (performed through separate tests) enables accurate estimation of EVM without the need for transmitting and receiving large number of data bits. This has the potential to significantly reduce the EVM test time.

2.2 BER TEST TIME REDUCTION FOR UWB DEVICES

In production test environment, UWB devices are characterized for BER in the presence of an external interferer. Production test techniques that employ the power of alternate test to reduce the BER test time are explored in this section for both pulse-based and MB-OFDM UWB devices.

2.2.1 Pulse-based UWB Communication

Wireless communication based on pulsed data transmission has the ability to provide high data rates when used as an overlay technology. A pulsed transceiver uses

very short duration pulses, typically of the order of nanoseconds for transmitting data. As the duration of the pulses is small, the spectral spread of the data is large. For this reason, this type of transmission scheme came to be referred as ultra wideband. In most cases, the pulses used for transmission are Gaussian pulses or their higher derivatives. The equations for both Gaussian pulse and its 2nd derivative are given by Equation (19) and Equation (20), respectively (Figure 26).

$$w(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(t-\mu)^2/2\sigma^2} \tag{19}$$

$$w''(t) = p(t) = \frac{1}{\sigma^3\sqrt{2\pi}} \left[\left(\frac{t-\mu}{\sigma} \right)^2 - 1 \right] e^{-(t-\mu)^2/2\sigma^2} \tag{20}$$

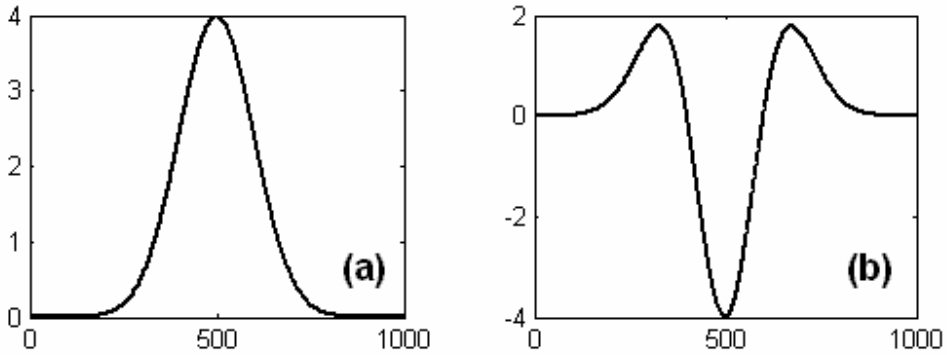


Figure 26 (a) Gaussian pulse and (b) its second derivative

2.2.1.1 Modulation Schemes

There are mainly two modulation schemes used in pulse-based transmission – bi-phase modulation (DS-UWB) and pulse position modulation (PPM), also known as TH-UWB, where DS and TH stand for direct sequence and time hopping, respectively. DS-UWB employs a transmission scheme where each bit is encoded using a spreading code that determines the time slot when the pulse is transmitted. The spreading code is kept unchanged for all the bits during DS-UWB transmission, while the polarity of the pulses

is changed depending on the transmitted bit. Thus, for a spreading code of length N bits and a baseband data rate of t_b, the pulse duration t_p can be expressed as $t_p = t_b / N$.

TH-UWB uses a more complex modulation scheme in which the pulses are transmitted at specific time slots based on the baseband data bits. Usually, N baseband data bits form the spreading code, and the pulse is transmitted in the time slot that is represented by the N-bit binary code. Hence, for baseband data rate of t_b, the pulse duration is given by, $t_p = t_b / 2^N$.

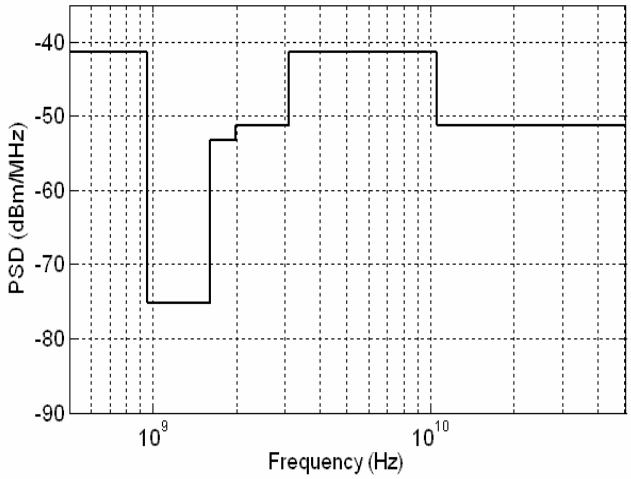


Figure 27 FCC Mask for UWB communication

Before transmission, the generated pulses are passed through a band pass filter, which shapes the pulses and limits any out-of-band emissions to satisfy FCC limits. The FCC PSD limit is shown in Figure 27. Very low PSD ensures that the pulse-based communication systems do not affect the quality of transmission of other standards. Among the many other pulses proposed for pulse-based transmission [84][85] , 2nd derivative of a Gaussian pulse, as shown in (2), fit the FCC PSD spectrum without the need for any filtering and is usually preferred in this communication scheme.

2.2.2 Pulse Generation

The biggest challenge in pulse-based transmission scheme is generation of Gaussian pulses and their higher derivatives and performing modulation on the continuous time-domain signal. Many such techniques have been proposed in the past. The earlier circuits were usually large in size and used very high power. This made them infeasible for integration in wireless devices. One such circuit uses spark plugs for pulse generation [86]. Other such methods use Schottky diodes, step recovery diode pulsers and coplanar waveguides [87]-[94]. Other improved methods were proposed in [95][96], where impulse-shaping network using metal semiconductor field effect transistors (MESFETs) were incorporated. Other such methods include generating pulses in the frequency domain and performing FFT on them prior to transmission [97][98].

Recently, many new techniques have been proposed for pulse generation using CMOS technologies. These can be classified into two groups, *(a)* direct generation of pulses and *(b)* generating pulses via up-conversion. Most of the techniques based on *(a)* try to perform pulse-shaping via filtering [99] and use delay/control signals to set the pulse width [100]-[110]. Typical pulse widths obtained from these range from 150ps – 1.2 ns. A more aggressive method is demonstrated in [111] based on MOS current mode logic (MCML). In this technique, the pulses are generated by a combination of specific input transitions on the control taps of a power amplifier. Some other methods used high-speed ADCs to generate such pulses [112]. In [113][114] up-conversion techniques are used to generate pulses from baseband. Some techniques have been proposed based on bipolar junction transistors (BJT) and BiCMOS technology [115]. Various design methods for designing the front-end components of pulse-based transmission have also

been proposed [116][117]. Few other novel techniques have also been proposed by various authors [118]-[122]. Overall, all the above methods indicate that pulse generation is a relatively easy task and different pulse shapes can be achieved without significant modifications to the generation circuitry. This knowledge is utilized in this work to alleviate the production testing process using a sinusoidal pulse generator instead of the standard Gaussian monocycles.

2.2.3 Receiver Architecture

The UWB receiver consists of a correlator, which is composed of an integrator, followed by a Sample and Hold (S/H) block, a comparator and finally a bit extractor, as shown in Figure 28.

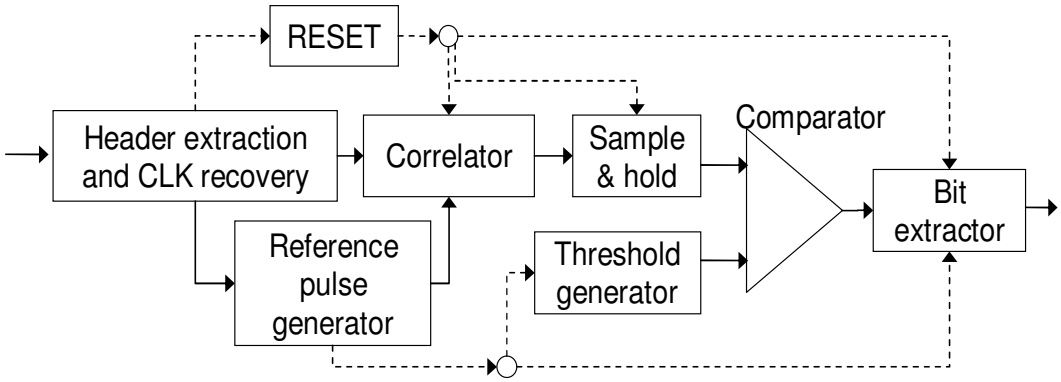


Figure 28 UWB receiver architecture

The receiver has a reference pulse generator (also called reference pulser) unit, which creates the transmitted pulses for bit '1'. Moreover, based on the modulation scheme used, the control signals for the threshold generator and the bit extractor are generated by the reference pulse generator. The received waveform is correlated with the reference pulser output over one bit duration (t_b) and the correlator output is sampled at specific

time points of the total bit duration. The correlator, S/H output and the bit extractor are reset after one bit duration. Thus, each received bit is independent of the previous bits.

For DS-UWB, the pulses for bit '0' and bit '1' have same shape, but are inverted with reference to each other. In this case, the reference pulses generated correspond to a '1' bit only and based on the correlator output, the received bit is decoded. Thus, if a '1' is received at the correlator input, the output at the end of one bit period is a positive value higher than the threshold, which is then sampled as a '1' by the receiver. If the received bit is a '0', the corresponding correlator output at the end of one bit period is negative, which is detected as a '0'. For TH-UWB, the transmitted bits and the reference bits have the same shape; hence the correlator output is always positive. However, bits are decoded by detecting the time period during which the correlator output reaches a high positive value and buffered in the bit extractor before sending to DSP.

2.2.4 BER Testing of Pulse-Based UWB Receivers

Due to the low-power operation of UWB devices, efficiency of reception at the receiver is severely affected by interference from other moderate-to-high-power narrow-band transmitters. For this reason, UWB receivers must be characterized and tested for bit-error rate performance in the presence of narrow-band interferers during manufacturing. Production testing requires a minimum number of bits to be transmitted and decoded at the receiver to compute bit errors in the presence of an interferer. The number of bits transmitted during the production test procedure is inversely proportional to the target bit error of the device. For low interference levels, bit errors are small (10^{-6}-10^{-10}), requiring a large number of bits to be transmitted for reliable testing. This results in long production test time and increases the overall manufacturing cost of the device

and may reduce profit margin considerably. So, it is necessary to employ new test techniques during production testing to reduce the time required to test the device.

For testing the receiver, the interference signal with a single tone since the signal bandwidth of the pulses is much larger compared to the bandwidth of the interfering signal. The following discussion assumes bi-phase modulation scheme and 802.11a WLAN interferer is used for transmission. However, the overall approach can easily be extended to transceivers employing pulse-position modulation and any narrow-band interferer. The WLAN signal is associated with a random phase $\theta(t)$ at 5.25GHz. The phase noise component of the signal is assumed to have a peak phase deviation $\theta_{pk} = 10°$, with a periodically varying phase term. The signal can be modeled as shown in Equation (21),

$$I(t) = A\sin(2\pi f_c t + \theta(t) + \theta_{pk}\sin(2\pi f_m t)) \qquad (21)$$

where A=amplitude of the interference signal, f_c = 5.25GHz, and $f_m = f_c/1000$.

2.2.4.1 Standard Test Method for Pulse-based Receivers

In the following discussion on the standard BER test method for pulse-based receivers, all analysis presented is done received bit with a logic value '1'. The proposed solution remains the same for bit '0'. In presence of interference and channel noise (assumed to be white gaussian noise), the received signal is

$$r(t) = p(t) + I(t) + n(t) \qquad (22)$$

where $p(t)$ is transmitted pulse, $I(t)$ is the interference and $n(t)$ is the noise contribution. The reference pulse generator generates a waveform similar to the one transmitted, which is correlated with the received signal, $r(t)$. Thus, the correlator output is given by,

$$c(t) = \int_0^{N\times D} \int_0^{t_p} r(t)R(t_p - t)dt \qquad (23)$$

$$= \int_0^{N\times D} \int_0^{t_p} p^2(t)dt + \int_0^{N\times D} \int_0^{t_p} I(t).p(t)dt + N(t) \qquad (24)$$

Here, $R(t_p - t)=R(t)$ and $p(t)=R(t)$ for $0 \leq t \leq t_p$, N is the number of bits transmitted, D is the length of spreading code.

Close observation of the above equation reveals that the first term is always positive for a bit '1' (negative for a bit '0'), irrespective of the pulse waveform used for transmission. Thus, for an error to occur for bit '1', the second term needs to be more negative than the first term (more positive for a bit '0'). If no interference is present ($I(t) = 0$), all the bits are correctly detected, and the error probability is 0. The probability of correct detection of '1' can be formulated as $p(1) = p[c(t)|_{t=tb} > 0]$. To obtain a closed form equation to estimate the probability of error for a bit in the presence of interference, Equation (24) must be integrated to find $c(t)$. While the first term of Equation (24) can be evaluated, the second term, which has the form

$$f(x) = \iint x^2 \sin(x) e^{-x^2} dx \qquad (25)$$

is not integrable. Thus, the only way to obtain an estimate of the error probability is to use numerical methods for integration. The *sample and hold* circuit samples $c(t)$ at $t=t_b$ to determine the value of the received bit. The random phase $\theta(t)$ in Equation (21) is a

uniformly distributed random variable and can take any value in (*0, 2π*). The variation in the sampled value at the instant $t = t_b$ for various phase values is shown in Figure 29.

In Figure 29, the decision boundary for detecting bits under bi-phase modulation is shown by a solid horizontal line. From the figure, the positive offset due to the first part of the integral in Equation (24) can be easily seen. It is evident from the figure that the higher levels of interference start causing bit errors as the sampled value starts taking negative values at certain phase values (the gray shaded portions in the plot), thus increasing the error probability. However, due to the unknown variables associated in Equation (22) and highly nonlinear nature of Equation (24), it is not possible to construct a direct linear relationship between *p(1)* and the interfering signal.

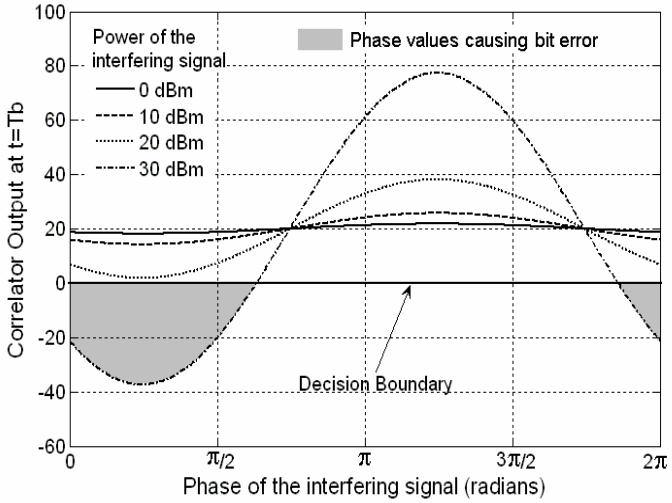


Figure 29. Variation in sampled value with change in phase of the interferer signal (for various power levels of the interferer).

2.2.4.2 Proposed Test Approach for Pulse-based Receivers

Testing the receivers for error probability at low interference levels using standard test procedure would require a large number of bits, and thereby long test time. The proposed method aims to adopt a strategy where the performance of the system can

be degraded systematically during testing – such degradation would result in worse BER specification value and a larger number of bits would be in error. This would reduce the test time as it would be necessary to measure only the elevated BER value during production testing and correlate the elevated BER value to the original value. This would reduce the overall test time significantly.

Moreover, the method needs to be non-intrusive, meaning that it would not be possible to make any changes within the device during testing – only possible changes that can be made are limited to the test stimulus and test setup. The focus then is on finding an alternate test stimulus that can elevate the BER within the same test setup. As indicated in the previous section, the correlator output has a positive offset for bit '1' (negative for bit '0') that prevents the output of the correlator *c(t)* to be detected erroneously in presence of small interference and noise. The easiest way to increase the BER is to reduce this offset, making the system more prone to errors. This offset is obtained by correlating two identical waveforms – using two different waveforms with little correlation would reduce this offset.

A waveform that is easy to generate during production testing and has small correlation to the gaussian pulses used in UWB is, therefore, a good choice . Such waveforms are limited to sinusoids, square or triangular pulses, or other Gaussian pulses used in UWB. From Figure 30 one can see that for such waveforms, the sampled value by the bit slicer varies considerably. For our discussion, the choice tends to select sinusoidal or triangular pulses as the sampled value is small at the end of the integration period. A sinusoid seems more favorable as it exhibits two benefits over triangular pulses: sinusoids are easier to generate in ATE and do not need any custom test program

to be written by test engineers, and sinusoids occupy much less bandwidth compared to triangular pulses. This reduces the effect of harmonics and does not saturate the receiver. Moreover, it is easy to generate sinusoidal pulses using a pulsed RF signal generator.

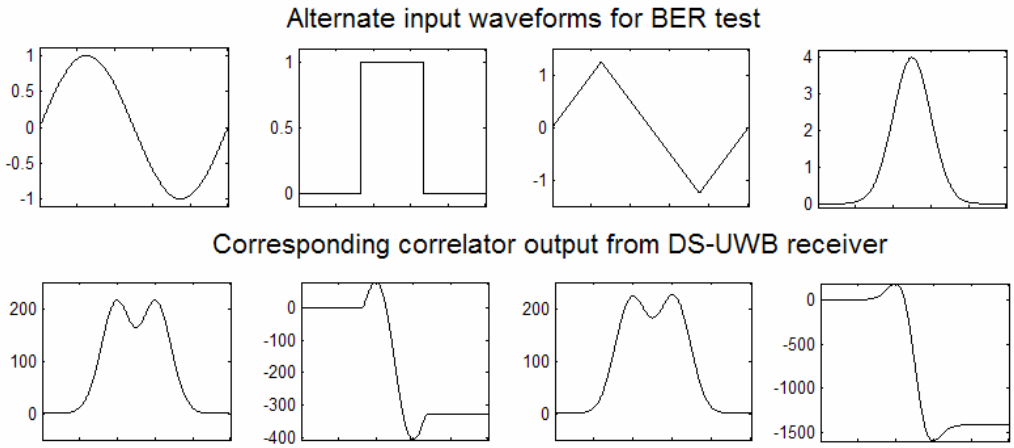


Figure 30 Possible input waveforms for BER testing

As per the above discussion, sinusoidal pulses were chosen as the alternate test stimulus for testing error probability. However, the frequency of the sinusoid needs to be carefully chosen so that the offset does not become zero (this might happen if the frequency of pulse and sinusoid are equal). This is evident from Figure 31 , where the variation in the correlator output is shown for different frequencies of the input sinusoid. Also shown are the ranges of the final sampled values for variation in input phase of the interferer and noise. The frequency of the sinusoid was chosen to be slightly larger than the pulse frequency, as the value sampled by the bit slicer exhibits larger variation for frequencies greater than the pulse frequency. For this work, the frequency was chosen to be 1.2 times the pulse frequency.

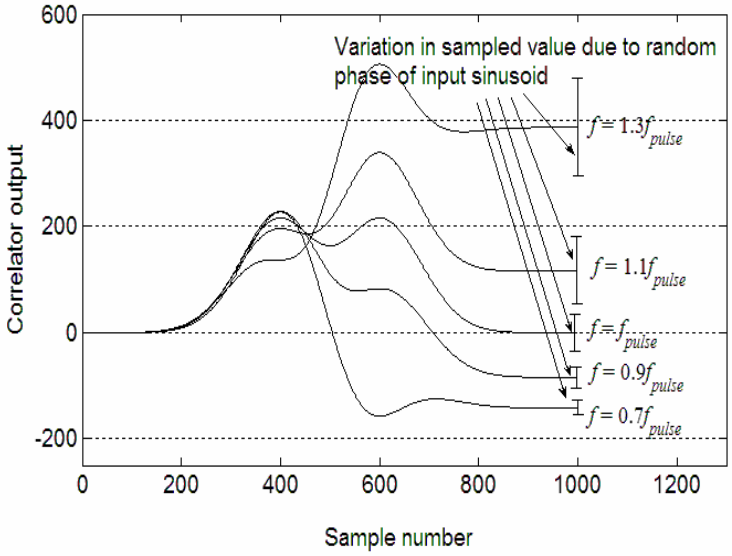


Figure 31 Variation in correlator output for various input sinusoids with different frequencies. Also shown are the ranges of sampled values for random phase values of the interferer and noise from the channel

For sinusoidal input pulses, Equation (22) changes to

$$r(t) = s(t) + I(t) + n(t) \qquad (26)$$

where, $s(t) = A\sin(2\pi f_p t + \phi)$. The sinusoid has a frequency f_p, and a fixed phase of ϕ (set to 0). This changes Equation (23) to (noise is ignored for simplicity)

$$c(t) = \int_0^{N\times D^{t_p}} \int_0 [s(t) + I(t)]p(t)dt \qquad (27)$$

$$= A \int_0^{N\times D^{t_p}} \int_0 2\cos[\omega_d t + \theta(t)]\sin[\omega_s t + \theta(t)]p(t)dt \qquad (28)$$

where $\omega_d = (\omega_c - \omega_p)$ and $\omega_s = (\omega_c + \omega_p)$.

If the frequency of the sinusoidal pulse $s(t)$ is chosen close to the interferer, then the cosine term is almost equal to unity during the pulse duration, giving a probability of

error of ~0.5 for all levels of interference, which is not desired. Thus f_p is chosen such that the variation in correlator output value due to change in phase has maximum peak-to-peak variation at $t = t_b$. The test setup is shown in Figure 32.

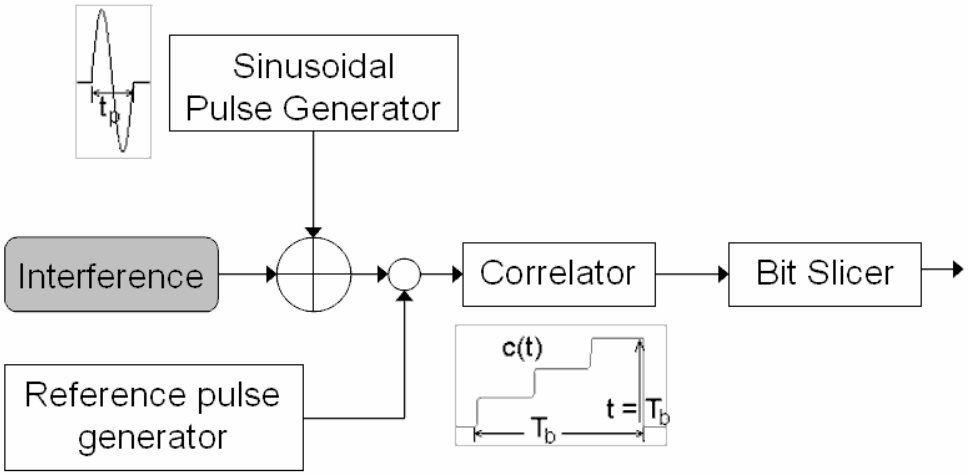


Figure 32. Proposed test architecture using a pulsed RF signal generator.

2.2.4.3 Simulation and Measurement Results

The results section presents a simulation study for bi-phase modulation with a *WLAN* interferer, followed by hardware measurements presented for pulse position modulated transceivers with a *Bluetooth* interferers. For hardware demonstration, the pulsed transceiver was implemented on an Altera programmable gate array development board (Stratix® II, ES280 series) and interferer signals were generated from a HP 4403B signal generator.

2.2.4.3.1 Simulation study – WLAN interferer

To demonstrate the proposed method for error sensitivity analysis of a pulse-based transceiver, transmitter and receiver models were developed first. Assuming a production test environment, the multi-path components that might appear in a

communication channel was ignored, and transmit-receive antennae were modeled as differentiators. In the simulation environment, the data rate was set to 83.33 Mbps, and pulse width of 500ps. When simulated without any added interference, all the bits were correctly decoded. If an interferer of sufficient power is added to the signal, bit errors start to occur and keep increasing as the interferer power is increased. Simulations carried out for a *WLAN* interference signal showed that a few bit errors were caused by the interferer.

Next, simulations were performed at various interference levels to find out how the bit error rate changes with E_b/N_0, where E_b is the energy per bit duration; N_0 is the total amount of noise power, including that contributed by the interference. Figure 33 shows the performance of a pulse-based transceiver in the presence of white Gaussian noise and varying power levels of interfering *WLAN* signal (graph *'A'*). Also shown in Figure 33 is the error probability for the proposed approach using sinusoidal pulses (graph *'B'*).

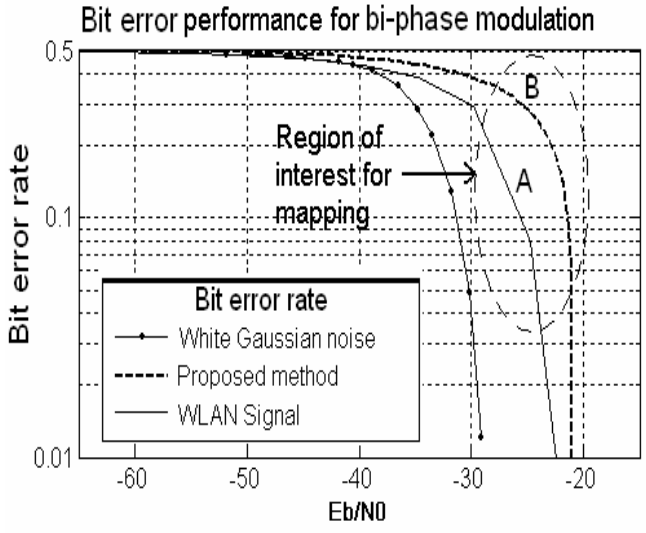


Figure 33 Bit error performance of a pulse-based transceiver in presence on interference.

Next, the measured error probability value using the alternate test stimulus (sinusoidal pulses) at low interference levels was mapped to the actual error probability value using correlation functions. Multivariate adaptive regression splines were used as the mapping function. This uses piecewise linear basis functions to create a mapping between multiple nonlinear datasets. A mapping function from graph *'B'* to graph *'A'* is developed. The mapping function takes the error probability value measured using the proposed technique as input and generates the actual error probability, for a fixed E_b/N_0 value. To develop the mapping function, first, the error probability for the pulse-based receiver is measured using the proposed technique. At the same time, the test is performed using the pulse-based transceiver, with sufficient number of bits (>100/*bit error rate*) to determine the exact error probability value (which requires a large number of bits and hence, longer test time). This is repeated at different power levels of the interfering signal. Finally, a mapping function was developed for the region of interest from one data set to the other, as shown in Figure 33. Using this mapping function, the alternate test results were mapped back to the graph 'A' (with the sinusoidal pulses) to obtain the actual bit error rate at low interference levels. This is shown in Figure 34 . TABLE lists the error probability values for various interference power levels, for the standard test method and the proposed test method.

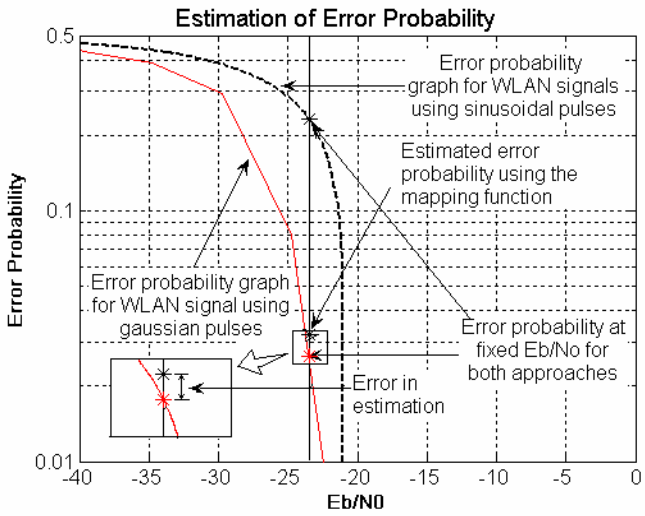


Figure 34 Estimating the error probability from the bit error rate curves.

TABLE 3 Comparison of simulation results for standard and proposed BER test methods.

SNR (dB)	***Test length***		***Test ratio***	***Accuracy***
	Standard test	**Proposed test**		
30	62,500	3,000	~21	10^{-4}
20	12,300	1,200	~10	2×10^{-4}
10	3,300	500	6.6	10^{-4}

2.2.4.3.2 Hardware case study

A pulse-based transceiver was implemented in an Altera development board and the proposed method was verified for *Bluetooth* and multi-tone interference signals. Pulse position modulation scheme was used in this case. The transmitted pulses were

looped back to the field programmable gate array device using the development board DAC and ADC pair. Using a signal combiner, the interference signal was added to the transmitted pulses. The frequencies of the interferer signals appropriately scaled down to be within the programmable gate array operating frequency range. The setup is shown in Figure 35. The simulation setup for baseband pulse generation is shown in Figure 36. The system was designed in Simulink/Matlab with custom DSP blocks from Altera DSP Builder. Using the setup, first the system was tested for BER performance under AWGN. No interference signal was added. The BER curve obtained for increasing noise level is shown in Figure 37.

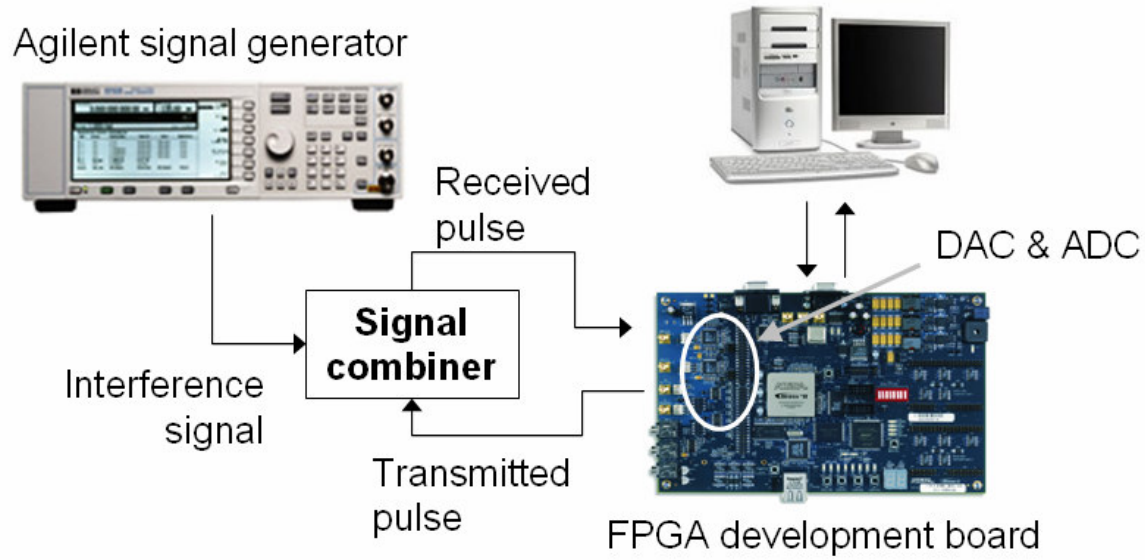


Figure 35. Hardware test setup for BER test.

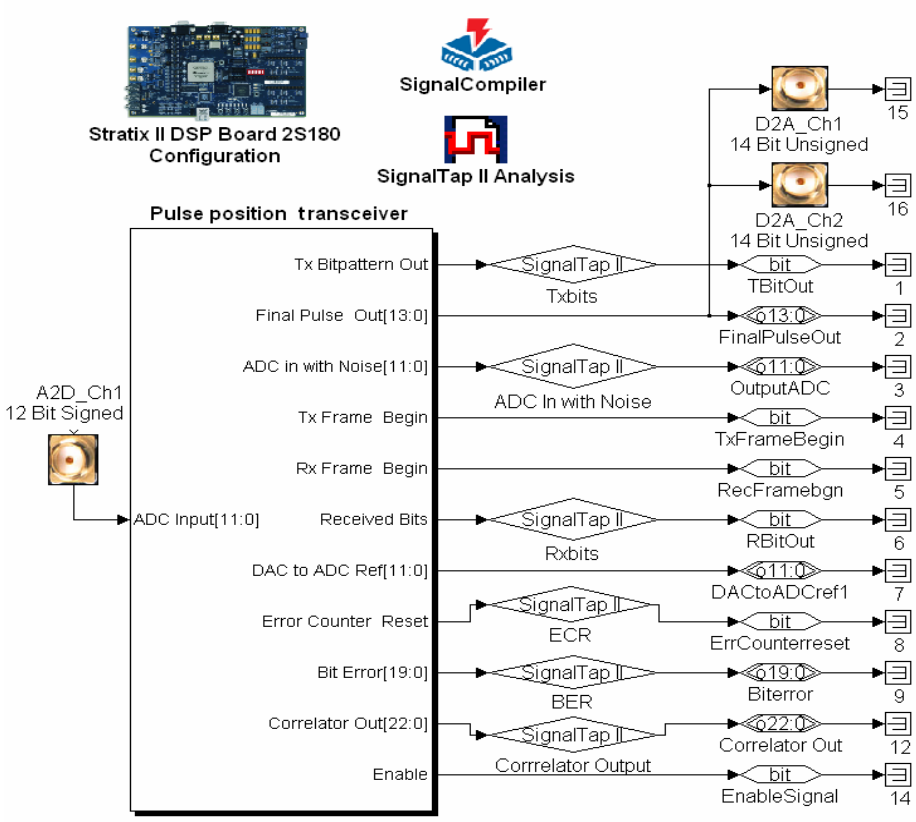


Figure 36. Top level schematic of Simulink test program developed for pulse generation, decoding and bit error rate computation.

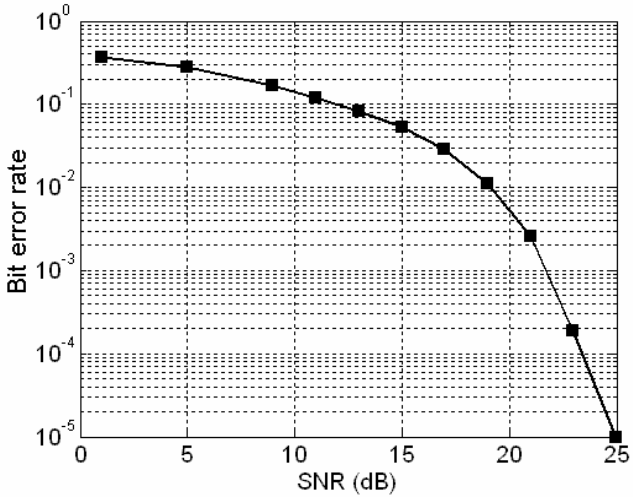


Figure 37. Bit error curve for white Gaussian noise only (no interferer).

Next, measurements to determine bit error rate were made in presence of *Bluetooth* interferer signal. This was generated from the signal generator and added to the transmitted pulse via the signal combiner. First, Gaussian pulses were used to measure bit error for various SNR values. At low interference levels, there were few or no bit errors, as is evident from Figure 38. However, as the interference power is increased, bit errors start to appear. This is shown in Figure 39, where few bit errors can be seen in the received bits.

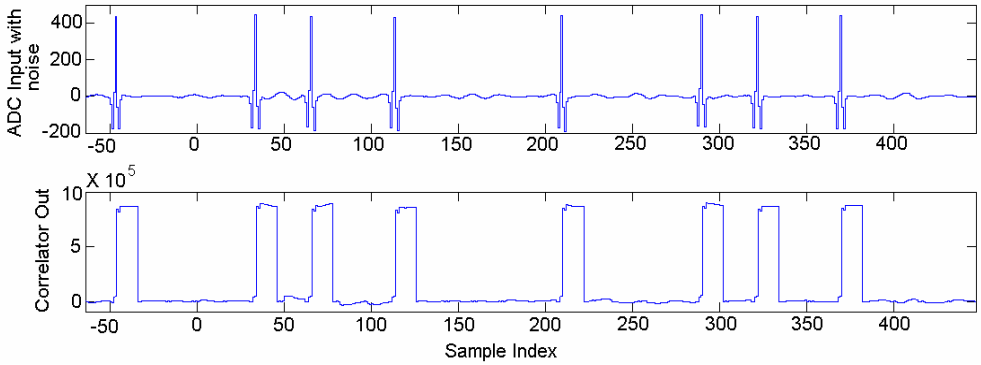


Figure 38. At low interference power, the correlator output is clean, and no bit errors occur.

Next, bit error was measured at various interference power levels by replacing the Gaussian pulses with sinusoidal pulses. For each SNR point within the knee region of the curve, a function was computed to map the elevated bit error values to the actual bit error values. At low interference levels, number of bits in error are much higher when sinusoidal pulses were used compared to standard Gaussian pulses. As seen from Figure 40 at low interference levels, BER is much higher when sinusoidal pulses were used compared to standard Gaussian pulses. Thus, time required to perform bit error rate measurements reduced significantly. Moreover, using the mapping function, actual bit error values could be predicted with an accuracy of <2%. The test lengths, obtained

speedup and test accuracy (for predicting from the mapping function) are listed in TABLE . The mapping procedure was limited to bit error rate values lesser than 10^{-}, as the bit error values for the standard and proposed method above 10^{-2} are comparable to each other and no significant test time saving can be obtained.

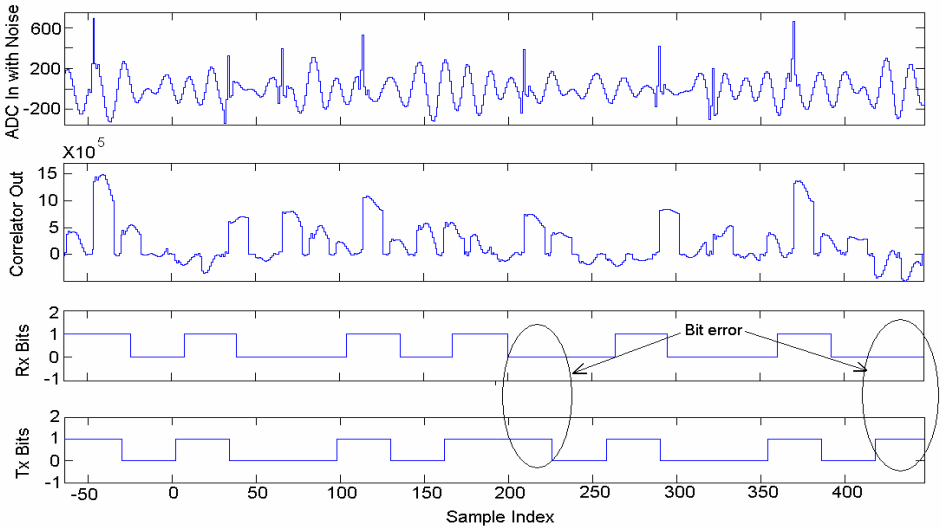


Figure 39. At a higher interference power, bit errors are observed in the received bits.

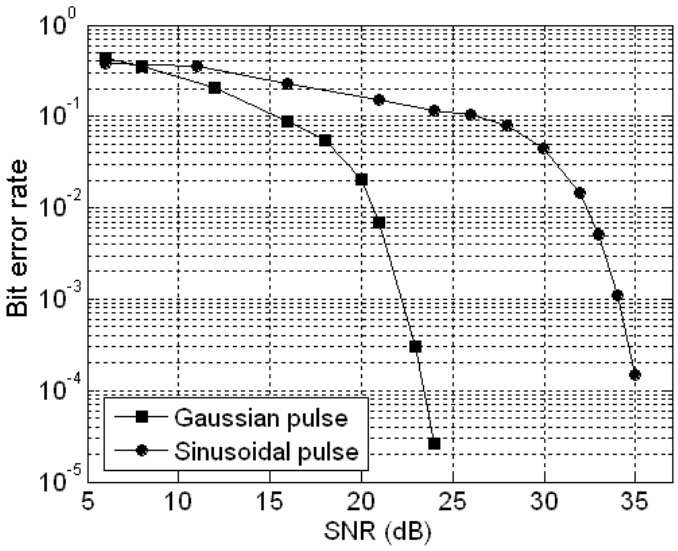


Figure 40. Bit error rate curves for Bluetooth interferer for Gaussian and sinusoidal pulses.

TABLE 4 BER performance for standard and proposed test in presence of *Bluetooth* interferer.

SNR (dB)	Test length		Test ratio	Accuracy
	Standard test	Proposed test		
24	1.906×10^7	4,266	4468	2×10^{-6}
23	1.641×10^6	3,927	418	3.5×10^{-5}
20	72,430	3,248	22	7.3×10^{-4}
19	24,050	2,719	8.8	2.1×10^{-3}
17	9,903	2,527	3.9	1.3×10^{-3}

The same experiments were repeated for a multi-tone stimulus, similar to that of an OFDM signal, used as an interferer. The BER plots for Gaussian and sinusoidal pulses show that the proposed technique elevates the BER at low interference levels, thereby reducing the test time. The details of the test procedure are given in TABLE .

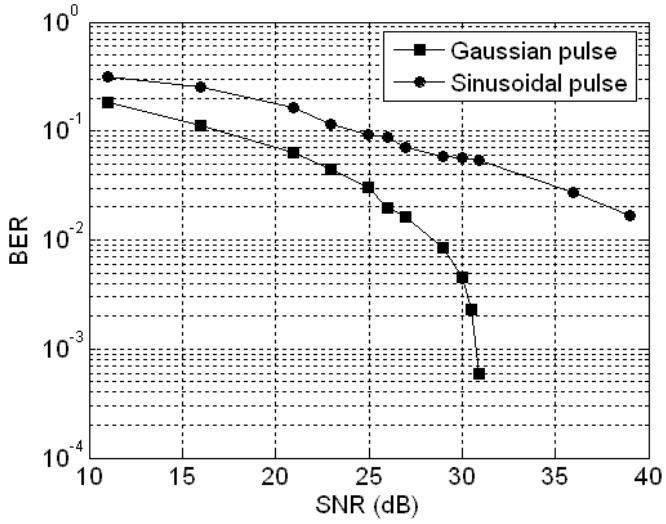


Figure 41 BER curves for multi-tone interferer for Gaussian and sinusoidal pulses

TABLE 5 BER performance for standard and proposed test in presence of *multi-tone* interferer

SNR (dB)	**Test length**		**Test Ratio**	**Accuracy**
	Standard test	**Proposed test**		
31	217,390	9,192	23.6	1.7×10^{-5}
30	110,109	8,834	12.5	2.3×10^{-5}
29	58,140	8,489	6.85	5.2×10^{-4}
27	30,864	7,153	4.3	1.03×10^{-3}
26	25,381	5,761	4.4	1.7×10^{-3}

2.2.5 Multi-band OFDM UWB

A production test approach for speeding up the bit-error rate test of MB-OFDM UWB devices is proposed in this section. The proposed method uses an alternate test stimulus, similar to the approach adopted for pulse-based UWB devices described in the previous section.

2.2.5.1 MB-OFDM Basics

The MB-OFDM PHY standard has emerged as another leading contender for adoption by the UWB community. MB-OFDM proposed for use by UWB systems is a variation of OFDM, used in WLAN (IEEE 802.11x). The UWB spectrum is divided into 4 band groups with each band further divided into 2 or 3 sub-bands, altogether yielding 14 bands, as shown in Figure 42. MB-OFDM uses a Time-Frequency code (TFC) to interleave data between the sub-bands in a band group. Transmitting data over this wide

frequency range further helps in increasing the robustness of the transmission to frequency-selective fading and interference from other sources.

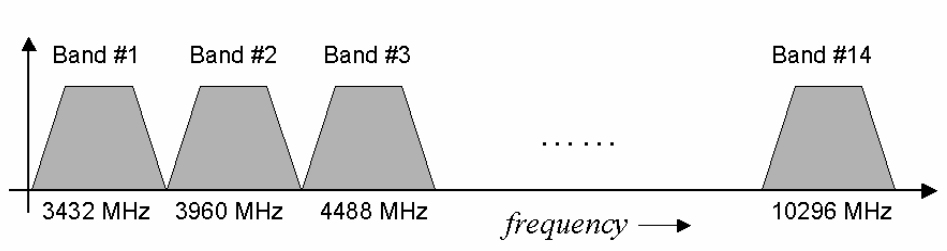


Figure 42. MB-OFDM Frequency allocation.

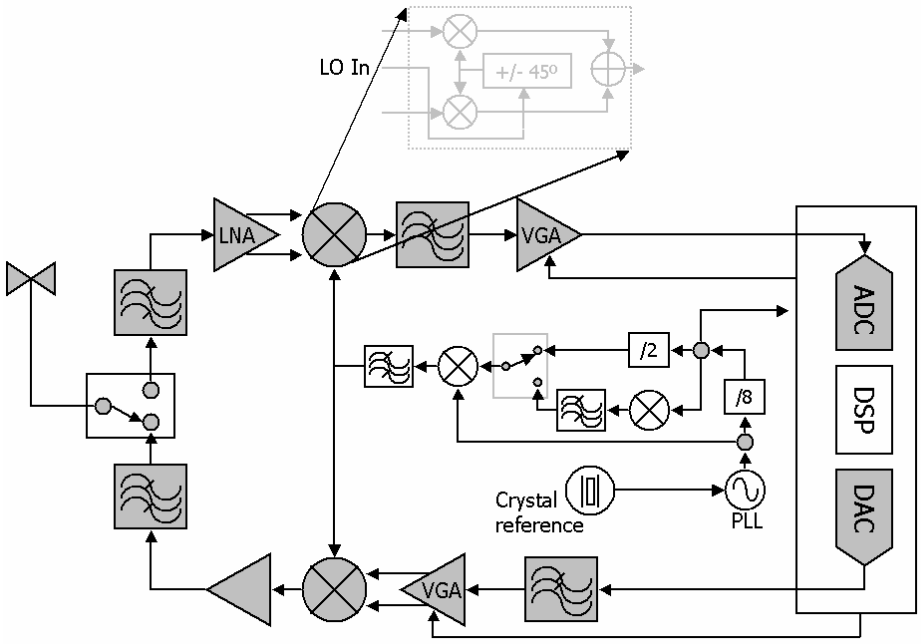


Figure 43. UWB transmitter architecture.

There are two main modules constituting the UWB transmitter: the digital module, which is usually a DSP and the *RF module*. The DSP takes the digital data bits as input, encodes and modulates them and passes on to the RF section through a DAC.. The RF module consists of a mixer and a time-frequency (TF) kernel that up-converts and transmits the data through the antenna. The UWB transceiver architecture is shown

in Figure 43 (the gray shaded blocks in the figure are modeled for test generation and validation purposes).

The TF kernel generates the LO frequencies to hop the transmitted signal from one band to the other. The hopping sequence is controlled by the digital block; every OFDM frame transmitted is up-converted using a different LO frequency in a different band. In Figure 43, the RF modules under test are shaded in gray. The UWB receiver has a similar TF kernel to down-convert the received signal. The hopping sequence is synchronized with the transmitter, based on the header and the preamble in each frame. After down-conversion, the signal is digitized and processed by the DSP block to recover the transmitted bits. The block diagram of a typical UWB receiver is shown in Figure 43. As shown in the inset, a pair of mixers with LO signals in quadrature are used and the signals are combined to generate the desired output.

2.2.6 BER Testing of MB-OFDM Transceivers

2.2.6.1 Standard BER Test Method

As in the case of pulse-based UWB transceivers, BER testing of UWB devices in production test involves transmitting a large number of bits from the BER Tester (BERT), transmitting the bits through the RF front-end system and receive the bits in the BERT. Finally, analysis is performed to obtain BER for the system. The BERT can transmit different patterns, introduce various errors (delay and jitter) and compensate for cable effects. A typical BER test setup using a BERT is shown in Figure 44. During production test, the interference signal is generated using a RF signal generator and is added to the signal using a power combiner.

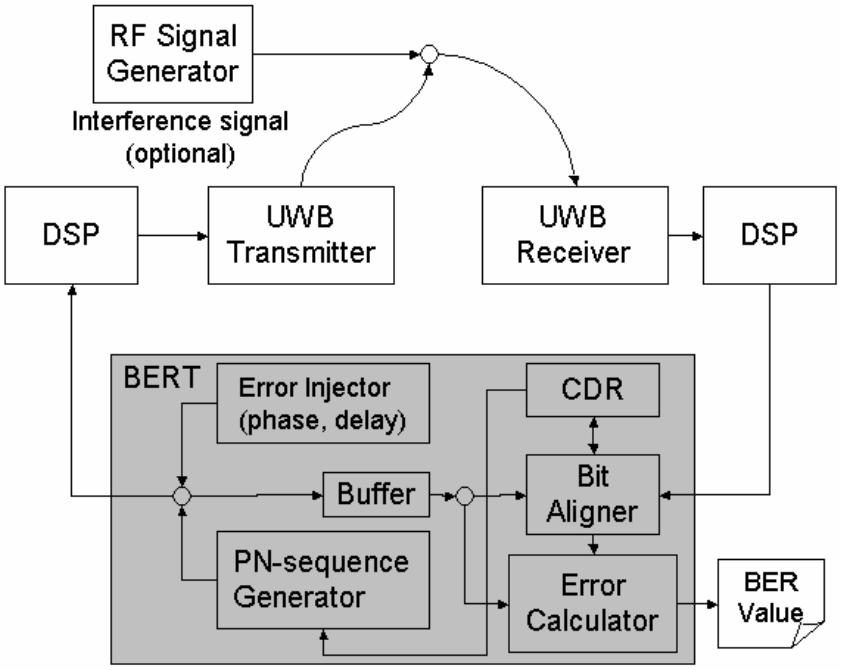


Figure 44. Standard BER test setup using a BER

2.2.6.2 Proposed BER Test Method

As the bandwidths of the interfering signals considered (Bluetooth, IEEE 802.11a and GSM 900) are much smaller than the bandwidth of the UWB signal (528 MHz), the interfering signals are once again modeled as a single tone. In the proposed test setup, a cabled connection used between the transmitter and receiver ensures repeatable results. The interference signal is modeled as a sine wave as explained in the previous section. A bit error is caused when a received QPSK symbol leaves the original quadrant's decision boundary and moves to a different quadrant.

The proposed BER test method modifies the phase relations between the QPSK symbols transmitted to increase the number of bit errors. By rotating the different symbols by different amount, the symbols are brought close to the decision boundary, thereby increasing the chances of bit errors. This method, as shown in Figure 45, can be

also applied in the opposite manner, where the symbols are rotated in opposite directions. As shown later, this increases BER considerably at low interference levels. This phase rotation does not change other system specifications such as EVM, as the transmitted and received vectors are both rotated by the same amount. In addition, the transmitted signal changes the time domain signal due to the phase rotation.

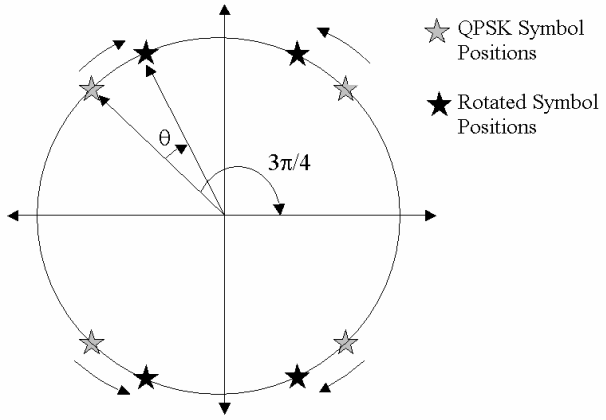


Figure 45. Rotated QPSK symbols for BER test.

The analysis for BER includes effects of "in-band" interference. The phase angle θ, shown in Figure 45, can be adjusted to control the BER at a specific interference level. A gradient search based algorithm developed determines the amount of phase rotation required to achieve a specific BER at very low interference levels. However, the phase rotation does not affect the BER when large interfering signals are considered. The proposed method uses smaller number of bits to test for BER, as rotating the QPSK symbols increases the number of error bits for a fixed number of transmitted bits. To determine the BER at low SNR levels, standard tests are first performed to measure the actual BER value at various interference levels (denoted by BER_a). Next, tests are performed using the proposed test method (denoted by BER_p). This BER value is used to estimate the actual BER value (i.e. without phase rotations), which is very small in

magnitude. To do so, a regression function is built between the actual BER values (BER_a) and BER values obtained from the proposed test approach (BER_p). During production test, the proposed test is performed (shorter test length) and the BER values are computed at different interference levels. These BER values are then input to the regression functions developed earlier and actual BER values are computed with a very high degree of accuracy.

2.2.6.3 . Simulation Results

For BER test, the phase offset is set to 25°. The BER tests were performed for three different interference signals: Bluetooth (2.4-2.4835 GHz), IEEE 802.11a (5.15-5.35 GHz) and GSM 900 (890-915 MHz). The results show that EVM and cumulative complimentary distribution function (CCDF) do not change by adding the phase offset to the transmitted data. CCDF is a common specification used to analyze the power statistics and is defined as the peak-to-average ratio of the transmitted signal [123].

2.2.6.3.1 . Bluetooth Interferer

The BER for MB-OFDM devices in presence of Bluetooth interfering signals does not reach a significant level due to the inherent low power levels of Bluetooth signals (Figure 46). As the maximum power level of Bluetooth signals transmitted is 0dBm, the interference signal power is varied from –40dBm to –10dBm. The EVM does not change considerably, as shown in Figure 47. The tests were performed by using the same bit sequence for the two tests. This shows that rotating the QPSK symbols does not statistically change the nature of the time domain signal and its peak-to-average ratio. The CCDF changes by 0.3% due to the phase offset.

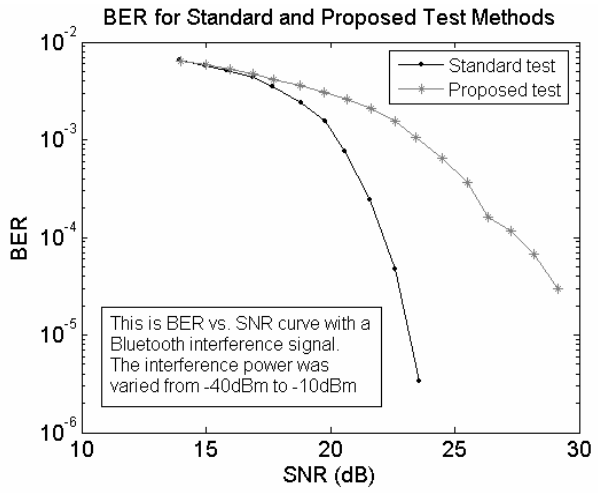


Figure 46. BER comparison for standard and proposed test for a Bluetooth interferer

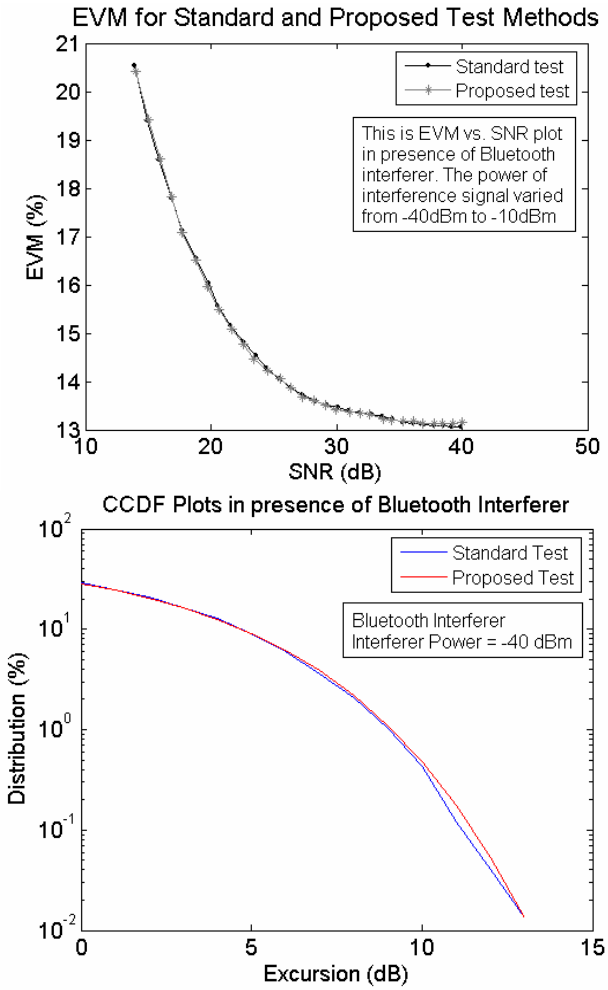


Figure 47. MB-OFDM Simulations: EVM and CCDF with varying SNR for standard and proposed test methods for Bluetooth interferer.

2.2.6.3.2 IEEE 802.11a Interferer

The IEEE 802.11a interferer is a stronger signal, thus resulting in a larger BER compared to Bluetooth. The plot of BER for increasing levels of interference signal power is shown in Figure 48. For IEEE 802.11a, the maximum allowable signal power for transmission is 15 dBm. In this work, the interference signal power is varied from -35 dBm to 5dBm.

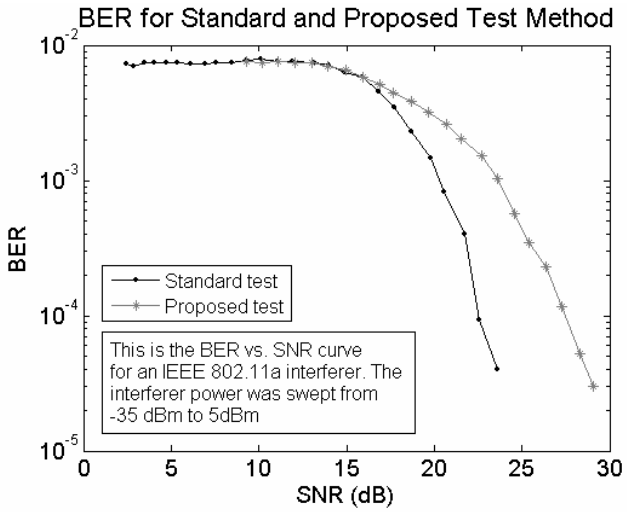


Figure 48 BER comparison for standard and proposed test for IEEE 802.11a interferer

The difference between the BER curves obtained using the standard test method for IEEE 802.11a (Figure 48) is evident from the figure. However, a closer look at the BER curves obtained using the proposed test approach shows that the curves have a similar nature. This is because the BER for both the systems is much larger (factor of 10 to 100) than the actual BER value. If we keep increasing the phase offset, at one point of time, the curves will be the same for different interference signals and the slope will be considerably low. This is intuitively true, because in such a case, all BER values will be in the close proximity of 0.5 at different SNR values.

The variation of EVM and CCDF for different SNR values for an IEEE 802.11a interferer is shown in Figure 49.

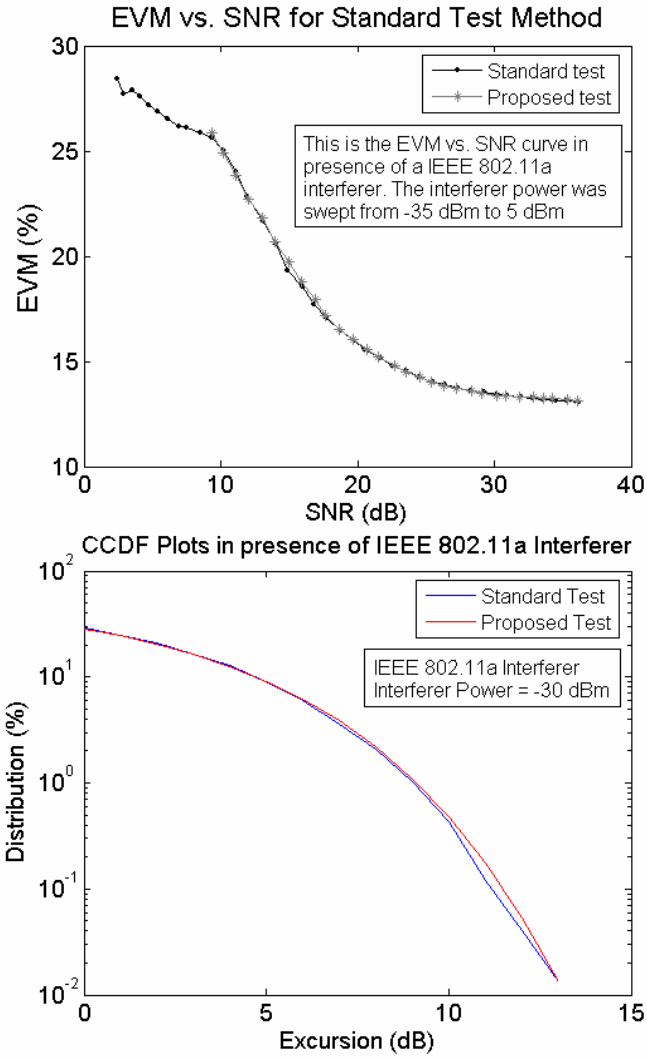


Figure 49 MB-OFDM Simulations: EVM and CCDF plots with varying SNR for standard and proposed test methods for IEEE 802.11a interferer

2.2.6.3.3 GSM Interferer

For GSM 900, the maximum allowable signal power for transmission is 10dBm. In this work, the interference signal power is varied from -40dBm to -15dBm. The plot of BER for increasing levels of interference signal power is shown in Figure 50.

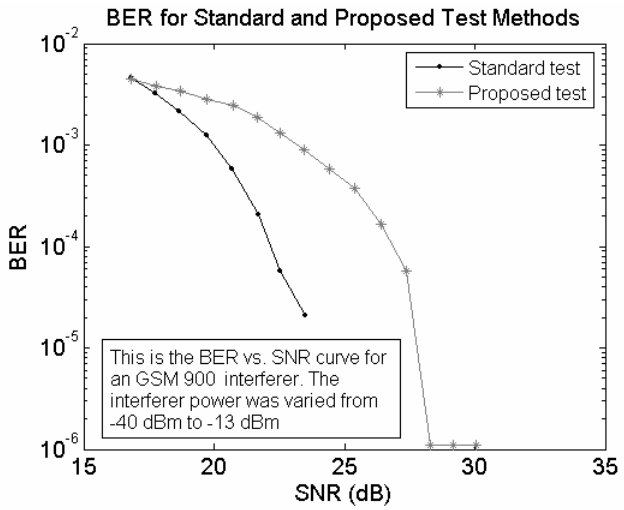


Figure 50 BER comparison for standard and proposed test for GSM 900 interferer

For the proposed test method, the GSM 900 interferer shows a different behavior compared to Bluetooth and IEEE 802.11a. This can be attributed to the fact that the signal frequency for this interferer is much lower than the actual operating frequency of the UWB OFDM system. This shows that OFDM modulation is resilient to low frequency signals. Figure 50 shows the variation of EVM and CCDF for standard and proposed test approaches with varying SNR values. TABLE and TABLE shows the test-time savings obtained for different standards at different interference signal levels. Up to 20X savings in actual test time can be obtained using the proposed test method (including test setup, test initialization times).

In conclusion, a production test method for efficiently measuring BER of OFDM UWB devices was presented. The proposed test method provide test-time savings and reduces overall manufacturing test cost. Simulation models for OFDM UWB transceivers were developed and were used for generating test methodologies. Non-linearity effects of the transceiver, i.e. phase noise of LO, DAC and ADC nonlinearities were also incorporated in simulations. The proposed method selectively rotates the

transmitted symbols to increase BER at low power levels of the interfering signal. Using a set of regression functions, the actual BER can be accurately determined with huge reductions in test time. Apart from reducing the test time, the proposed method can be implemented on a low-cost ATE in a production test environment.

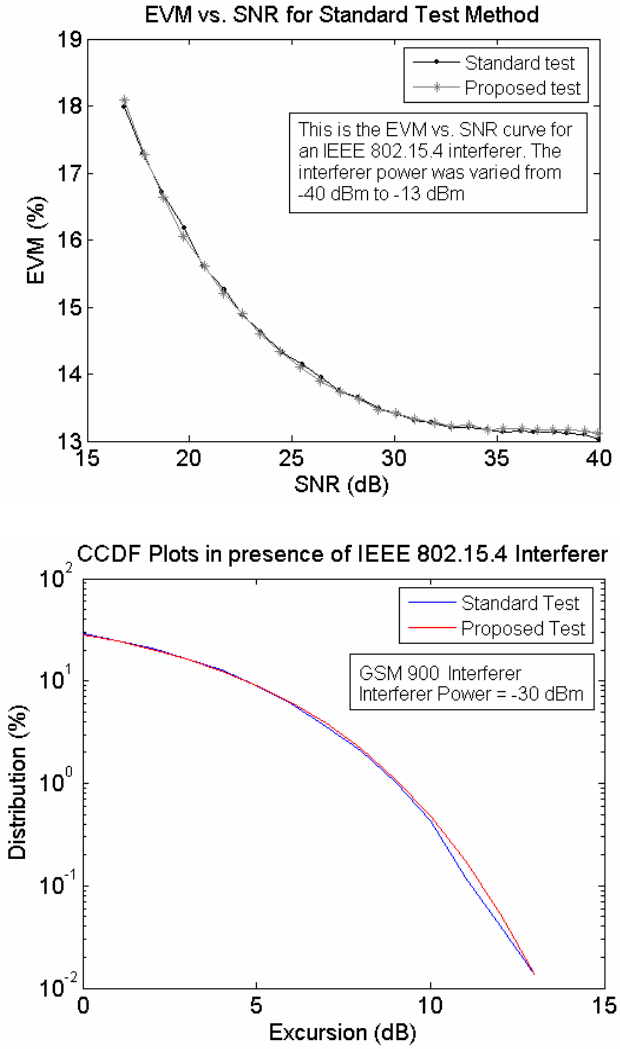


Figure 51 MB-OFDM Simulations: EVM and CCDF with varying SNR for standard and proposed test methods for GSM 900 Interferer

TABLE 6 MB-OFDM Simulations: Test-time savings for BER = 0.001

Interference signal	**Test length**		**Test Ratio**
	Standard Test Method	**Proposed Test Method**	
Bluetooth	40000	500	80
IEEE 802.11a	35000	700	50
GSM 900	22000	1000	22

TABLE 7 MB-OFDM Simulations: Test-time savings for BER = 0.0001

Interference signal	**Test length**		**Test Ratio**
	Standard Test Method	**Proposed Test Method**	
Bluetooth	400000	1500	267
IEEE 802.11a	350000	2500	140
GSM 900	220000	3300	67

Chapter 3

DIAGNOSTIC TESTING AND COMPENSATION OF RF TRANSCEIVERS

Wireless circuits are widely integrated into present-day consumer electronic devices (WLAN chipsets, UWB, Bluetooth etc.), and this trend is expected to continue in future. Low cost and reliability is crucial to success of the products in the marketplace. As semiconductor devices are increasing in complexity and shrinking in dimensions, variations in manufacturing process parameters have become a concern. This increased process variability in scaled semiconductor technologies, has increased manufacturing yield. Moreover, the operational reliability of the manufactured devices that pass production testing is of concern in the face of increasing process variability. Further, continually changing environmental factors like temperature, multi-path effects, interference, and device wear-out affect the operation of wireless systems in field. This is particularly important in the context of multiple high-bandwidth wireless devices operating in close proximity to each other. In such circumstances, it is necessary to incorporate on-chip wireless built-in self-test, and circuit adaptation techniques to compensate for circuit-level imperfections during the manufacturing phase as well as perform tuning during device operation in the field.

Compensation for manufacturing process variations and run time effects through tuning of RF front-end and baseband parameters is presented in this chapter for increasing the reliability of wireless systems. Due to the nature of transmission in

portable wireless transceivers, magnitude and phase of the received signal changes continuously. In the past, compensation and adaptation has been difficult due to the inability to measure deviations of RF circuit specifications using on-chip test mechanisms. While it is possible to test whether a circuit meets all its design specifications using complex external test instrumentation (RF stimulus generators, high-frequency RF measurement devices), it is not possible to measure all the design specifications of an RF circuit on-chip easily for adaptation and compensation. Current RF BIST techniques target one or a few RF design specifications, and are difficult to implement on-chip. In the proposed approach, diagnostic testing of the transceiver is performed using sensors in the RF front-end and transmitter-receiver loopback techniques. The information gathered is then used to estimate system-level specifications and dynamically tune the system for improved performance and increased operational efficiency. Diagnostic testing and compensation procedures mentioned in this chapter are performed either during the production test phase or during field operation of the device.

The emergence and advances in system-on-chip (SoC) technologies have seen different RF devices/modules integrated into a single chip/package. A standalone RF transceiver system is used to perform the functionalities of both transmission and reception of the RF signals. Most present-day wireless devices have an associated on-board DSP processor to process circuit data, and to serve as the interface between the circuits and the application layer. The DSP processor allows implementation of self-testing procedures and digital closed loop compensation schemes for optimal self-calibration of the transceiver. A hybrid compensation scheme that exploits tunability in RF section together with intelligent DSP-based algorithms is necessary towards

increasing the performance under significant process variations and environmental deviations.

3.1 OFDM TRANSMITTER TESTING AND COMPENSATION

In this section the proposed methodology to test and tune RF transmitter front-ends is described. PAs are an essential component in the transmitter of wireless communication systems. They are required to boost the transmitted signal power to increase coverage. Due to the high gain specification of the PAs, they are inherently non-linear. In order to achieve high power efficiency, the PA is often operated close to the saturation region, where it exhibits significant nonlinear characteristics including amplitude distortion (AM/AM conversion) and phase distortion (AM/PM conversion) of the input signal. Such phenomena not only corrupt the input signal but also introduce intermodulation distortions between neighboring frequency bands. It is therefore important to track the transmitter performance for non-idealities (diagnosis) and perform compensation to satisfy system specifications. A methodology that enables the diagnosis of PA operation for compensation is proposed in this section. The proposed scheme uses a built-in envelope tracking sensor at the output of the PA. The detector captures the envelope of a multi-sine test stimulus, and '*features*' extracted from this envelope are used to track the power and non-linearity specifications (amplitude and phase distortion) of the PA. The stimulus generation is enabled while the system is idle or could be a part of the training symbol employed during real-time communication. The envelope detector consumes very little area overhead and is more robust to process variations compared to other semiconductor devices. The captured envelope is a low-frequency signal that contains information about the non-linear properties of the PA. This information is then

used to estimate the specifications of the transmitter using alternate test framework. It is also used to tune the transmitter for non-idealities using two different approaches as described later in this section.

3.1.1 Behavioral Modeling of the Transmitter

Behavioral modeling has been extensively used to characterize PAs as it offers a convenient way to study the non-linear properties without the need for complex transistor-level simulations. Considerable volume of work has been done on the PA modeling [126]. Non-linear dynamic modeling approaches such as neural networks [132] and Volterra models [133] have been developed that accurately address both non-linear and memory effects in the PA. A simple behavioral model for the PA, based on the AM-AM and AM-PM distortion specification is used here for demonstrating the test and tuning concept. The two equations that describe the model are given by

$$A(r(t)) = \frac{\alpha_1 r(t)}{1 + \alpha_2 r(t)^2} \qquad (29)$$

$$\phi(r(t)) = \frac{\beta_1 r(t)^2}{1 + \beta_2 r(t)^2} \qquad (30)$$

where *A(r(t))* represents the non-linear amplitude-to-amplitude (AM/AM) modulation conversion, $\phi(r(t))$ is the amplitude-to-phase (AM/PM) modulation conversion, and *r(t)* is the normalized amplitude of the input signal. Typical values of the coefficients reported in literature [125] are $\alpha_1 = 2.0$, $\alpha_2 = 1.0$, $\beta_1 = pi/6$ and $\beta_2 = 1.0$. The Equations (29) and (30) relate the sampled input and output signals, and hence the model renders itself for analysis using realistic input signals. If the input signal to the PA model is given by

$$x(t) = r(t)e^{j\theta(t)} \qquad (31)$$

where *r(t)* and *θ(t)* are the amplitude and phase of *x(t),* respectively, the corresponding output y(t) is

$$y(t) = A(r(t))e^{j[\phi(r(t)+\theta(t)]} \qquad (32)$$

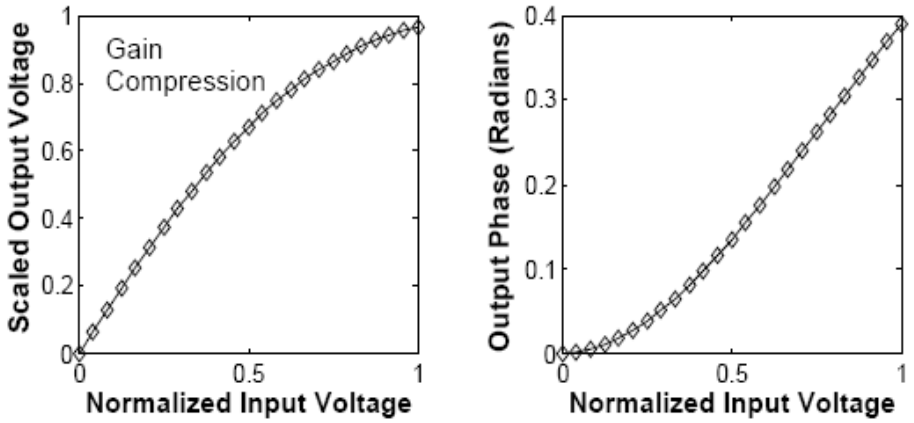


Figure 52 Amplitude and phase non-linearity in power amplifiers

The effect of AM/AM and AM/PM distortion introduced by the model is shown in Figure 52. At low input power levels, the output power increases linearly with the input power. However, as the input power increases, the PA gain starts decreasing, and is eventually driven into saturation. Additionally, the AM/PM modulation is also observed, where the output signal undergoes a phase addition that is consistent with Equation (30). These characteristics distort the signal envelope of the transmitted signal, introducing symbol errors in communication systems. Transmitters employing modulation schemes such as OFDM, CDMA etc. are particularly sensitive to these distortion effects due to the high peak-to-average (PAR) ratios of their signal envelopes.

The mixer of the RF subsystem is modeled as a non-linear transfer function followed by an ideal multiplier. The non-linear transfer function was realized as given by

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \qquad (33)$$

where α_0 = DC offset, α_1 = small signal gain, α_2, α_3 = non-linearity coefficients are used to realize the linear (gain) and non-linear (harmonics and inter-modulation terms) effects of the amplifier. The frequency mixing operation is realized by the multiplication operation.

$$y(t) = C \,.\, x_1(t) \,.\, x_2(t) \qquad (34)$$

where *C* represents conversion gain of the mixer. The local oscillator is modeled using Equation (35). Here, $A(t)$ is the amplitude of the signal and $\theta_{noise}(t)$ is the phase noise component of the signal. $\theta_{noise}(t)$ is a gaussian random signal with a peak value of 5°.

$$LO(t) = A\sin(2\pi f_c t + \theta_{noise}(t)) \qquad (35)$$

3.1.2 Testing and Diagnosis

A built-in envelope tracking sensor at the output of the transmitter is used to capture the response. The envelope detector consumes very little area overhead and preliminary simulations indicate its robustness to process variations [135]. The sensor captures the envelope of a multi-sine test stimulus, and 'response-features' extracted from this envelope are used to track the power and non-linearity specifications (amplitude and phase distortion) of the power amplifier (PA). The transmitter can be tested during production testing, or while the system is idle (concurrent testing). The captured response is a low-frequency signal that contains information on the non-linearity of the PA, is sampled, and fed into the baseband processor. The performance parameters of the transmitter can be predicted accurately from analysis of the obtained response envelope using non-linear regression mapping functions built from calibration

experiments. This is similar to using alternate test techniques for specification prediction. As in the case of alternate test, it is assumed that the devices under consideration are fault-free.

It is desired to efficiently estimate the linearity metrics of the transmitter from the response captured at the output of the envelope detector. A good test stimulus should therefore sufficiently exercise the non-linearities in the PA. A simple stimulus comprising of two arbitrary tones, one each for I and Q, and with sufficient amplitude to exercise PA non-linearity was used for diagnostic testing of the transmitter. In practice, when multiple non-idealities (I/Q mismatch, frequency offset) are present in the transmitter, a test stimulus optimization algorithm is required to increase the accuracy of prediction. The test response of a set of 100 different PA instances is shown in Figure 53. The captured test responses contain sufficient information (AM-AM & AM-PM) to estimate the non-linear parameters of the PA. A simple explanation for this is given below. If the baseband test stimulus ($X_{test}(t)$) is of the form

$$X_{test}(t) = a(t) + j * b(t) \qquad (36)$$

and, up-conversion to the RF band is performed by multiplying the signal with carrier ($c(t)$),

$$c(t) = \cos(w_c t) + j * \sin(w_c t) \qquad (37)$$

the corresponding output ($X_{RF}(t)$) is given by

$$X_{RF}(t) = \{a(t)\cos(w_c t) - b\sin(w_c t)\} + ... \qquad (38)$$

$$+ j\{a(t)\sin(w_c t) + b(t)\cos(w_c t)\}$$

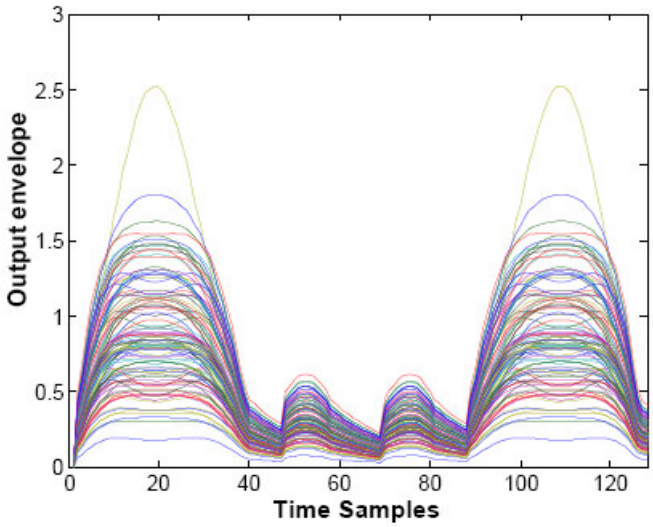


Figure 53 Envelope response for different PA instances

The complex envelope of $X_{RF}(t)$ as seen in Equation (38) is modulated by the baseband I-Q information. Any non-linearity introduced by the PA corrupts this envelope, and thereby, modifies corresponding baseband I/Q data set ($a(t)$, $b(t)$) to a new set of values ($a'(t)$, $b'(t)$). This information can be extracted by sampling the response with a low-speed ADC. The behavioral parameters α_1, α_2, β_1 and β_2 of the PA are estimated from the output response to a test stimulus. A set of 20 perturbed PA instances are used for evaluation. The estimated parameters are plotted against the actual values in Figure 54. As seen from the plots, these parameters are predicted with good accuracy.

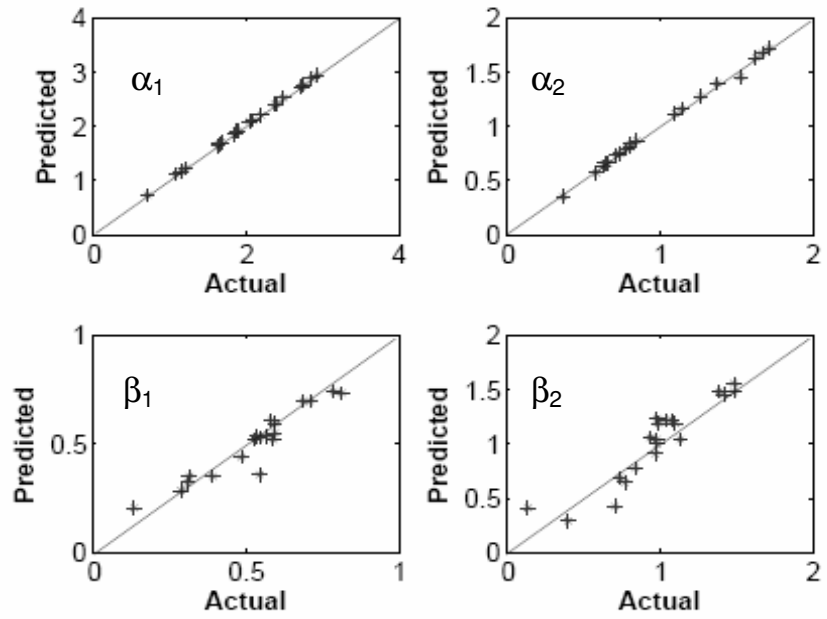


Figure 54 Parameter estimation using alternate diagnostic testing

3.1.3 Transmitter Linearization and Tuning

Due to the requirements of high-power efficiency, linearity and low-cost operation of transmitters in modern communication systems, research on efficient linearization techniques has assumed much importance [124]-[134]. Predistortion is a common technique that has been used widely for linearization. The predistorter creates a complimentary non-linearity in the baseband that is an inverse of PA non-linearity such that the overall transfer function of the system is approximately linear. The transfer characteristics of the predistorter, however needs to be tuned to the performance of every individual transceiver for "perfect compensation". The predistorter characteristics can be tuned in an adaptive (via iterative tests on the transceiver) or non-adaptive (via a single test on the transceiver) manner. In adaptive online tuning, the output of the PA is down-converted, de-modulated, and fed back to the baseband processor using the internal receive chain. The performance of the PA is continuously monitored and the predistorter

is tuned using search techniques based on least squares (LS) [131] or recursive least-square (RLS) algorithms [125].

A digital predistorter operates on baseband input signals to yield output signals that are precisely distorted in a complimentary fashion to the distortion produced by the PA. If the amplitude and phase operations performed by the predistorter are denoted by ∇ and Ψ, respectively, the output of the predistorter *p(t)* for an input signal *x(t)* is then given as

$$p(t) = \nabla(r(t))e^{[\theta(t)+\psi(r(t))]} \qquad (39)$$

For complete neutralization of amplitude and phase distortion introduced by the PA, the following equalities must hold

$$A\{\nabla(r(t))\} = kr(t) \qquad (40)$$

$$\phi\{\nabla(r(t))\} = -\psi(r(t)) \qquad (41)$$

where *k* is the gain of the PA. A key assumption made in the above equations is that the amplifier is memoryless, implying that the output is only a function of the instantaneous input. Complex modeling approaches are needed for incorporate memory effects of PAs. The digital predistorter is usually deployed in the final stage of baseband processing, prior to up-conversion and amplification.

The drawback of this approach is that the non-ideal effects of the receiver chain such as LNA non-linearity, I/Q mismatch etc. affect the calibration of the predistorter. A linearizing scheme implemented using this approach may not function effectively when the transmitter is communicating with a receiver in another transceiver device. The convergence speed of these adaptive algorithms is also an issue in certain applications. Adaptive linearizing schemes that use transmit-receive loopback are not effective as

process variation effects on receiver performance can lead to incorrect calibration of the predistorter-PA chain. Therefore, a technique that does not rely on the receiver path for feedback is more suitable. Moreover, the speed with which accurate transceiver tuning can be performed (adaptive or non-adaptive) is important for applications in which the transceiver adapts dynamically to changing operating conditions.

In a non-adaptive tuning approach, a one-time calibration of the predistorter transfer-function is performed during production testing. Each PA in the production line is tested and calibrated 'on-the-fly' using digital control signals from the automatic test equipment (ATE). To enable this, high-performance RF test equipment is required, increasing the manufacturing test cost. Another drawback of this approach is its inability to track and compensate for variations in PA characteristics *in the field* caused by temperature drift, device wearout etc.

3.1.3.1 Inverse Correction

To enable online tuning of RF transmitter systems, a BIT-based inverse correction procedure is proposed in this section. Once the system non-linearity metrics are estimated using envelope detector-based test as described in Section 3.1.2., the information can be used to modify (pre-distort) the transmitted baseband signal. The predistortion is performed by conditioning the signal using an inverse of the transmitter transfer function. This procedure is illustrated in Figure 55. The above mentioned procedure has a good potential to perform very good compensation of the transmitter for non-linearity and distortion. The compensation though is dependent on how well the transmitter specifications can be tested and the accurate estimation of the diagnostic parameters.

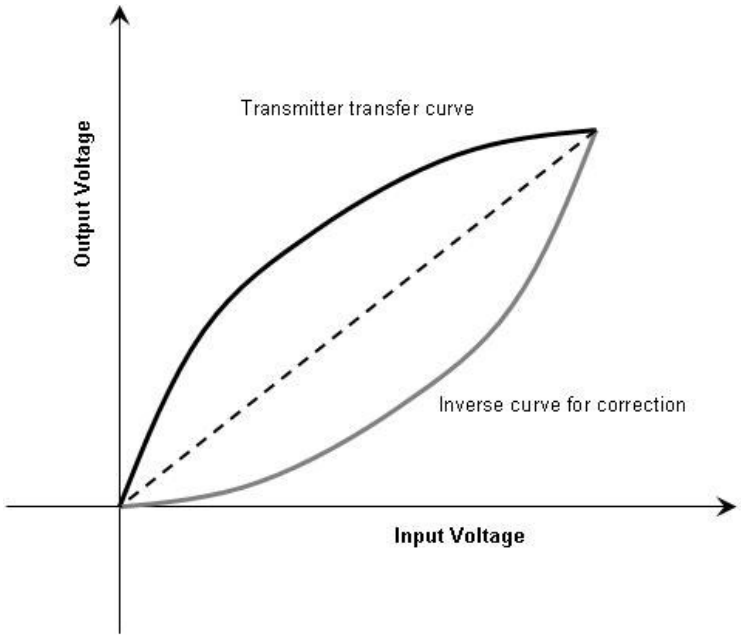


Figure 55 Inverse compensation for transmitter non-linearity

3.1.3.2 Adaptation Framework

Inverse correction can also be done using adaptive linearization to correct for AM/AM and AM/PM characteristics of the amplifier through indirect learning. The adaptive linearization is implemented using algorithms such as LMS, LS and RLS where feedback is used to train the amplitude and phase filter coefficients.

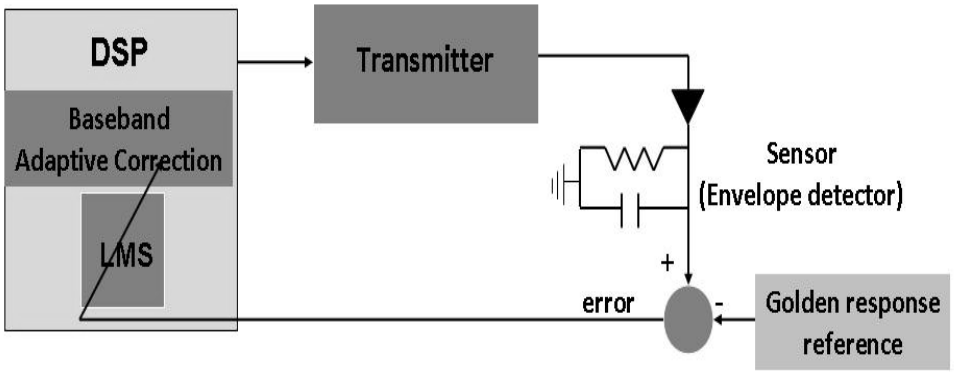


Figure 56 Adaptive Correction

Such adaptive schemes are an integral part of the baseband processing in present-day transceivers. The LMS algorithm, for example works by trying to minimize the LMS error between the filter output response and the desired ideal signal. In this case, an LMS-based tuning approach is implemented on the OFDM modulated output signal from the transmitter. The output signal is fed into an envelope detector and the resulting output is compared against an ideal golden response. The LMS filter is run to minimize the error by tuning the filter coefficients. The choice of initial filter coefficients is arbitrary. The procedure is illustrated in Figure 56.

3.1.3.3 Proposed Hybrid Approach for Transmitter Tuning

To increase the efficiency of predistortion, it is proposed to use an adaptation algorithm like LMS in combination with alternate diagnosis and inverse correction for improved results. As observed from simulation results (shown later), such an hybrid approach is effective in fine tuning the transmitter for improved linearity and increased efficiency. The power efficiency of the PA is determined by its bias condition, and low bias operation causes the device to operate at a reduced DC-to-RF power conversion efficiency. Digital predistortion can be used to increase the power efficiency of the PAs while maintaining the overall transmission quality (linearity). The proposed methodology for power-efficient and linear operation of PAs is proposed later in this section. The tradeoff between power efficiency and linearity of the PA is studied first using circuit-level simulations.

A PA was designed in 20um x 30 um silicon-germanium (SiGe) technology. The schematic of the PA is shown in Figure 57. It consists of two stages, the driver and the power stages in common emitter configuration, input/output and interstage matching

networks, and bias current sources to the two stages respectively. The parasitics associated with the bond wires in the RF signal path, supply and ground connections are included in the schematic to make it more realistic description of a practical device.

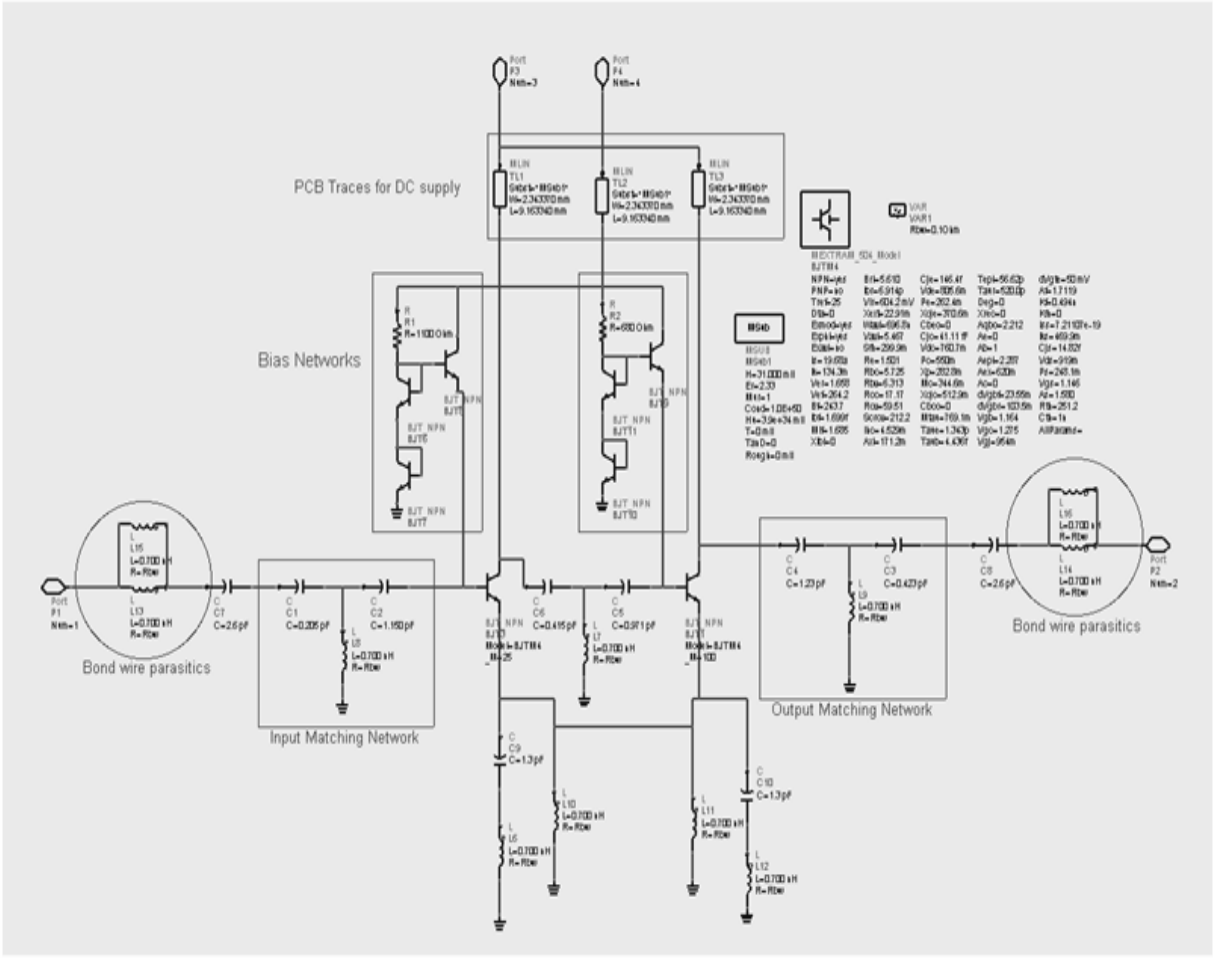


Figure 57 Two-stage power amplifier used for running bias vs. efficiency/linearity simulations

The PA is comprises two stages with a cumulative linear gain of a 27dB. The 1dB compression point is about 25dBm, and the output saturation power is around 29dBm. An important tradeoff in design is the one between the efficiency and linearity specifications. Figure 58 plots the variation of PA linearity and power efficiency metrics with varying bias voltages. At lower bias values, it is observed that the PA is more linear

but has a low power efficiency, and vice versa. A set of curves for efficiency and linearity can similarly be obtained by perturbing different process parameters. The PA gain response and power efficiency are, therefore, inherently non-linear functions of the process parameters and bias voltage.

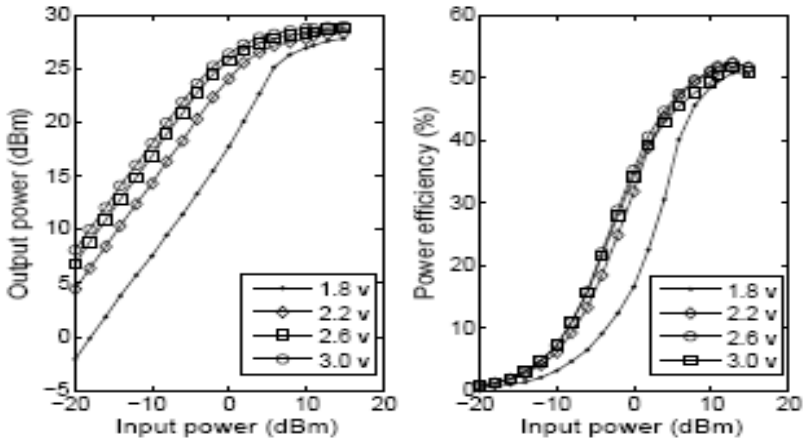


Figure 58 Power amplifier output power and efficiency curves for different bias voltages from ADS simulations

Figure 59 illustrates the proposed hybrid tuning approach. In the proposed approach, alternate test based inverse correction is performed in conjunction with adaptive predistortion for fine tuning the transmitter. Alternate diagnostic testing is used to additionally predict the initial LMS filter coefficients in addition to the transmitter behavioral parameters. As shown later, this helps in faster convergence of the LMS iterations. Moreover, with adaptive bias control, the transmitter can be operated at high efficiency while not compensating on linearity. The proposed approach is demonstrated using MATLAB simulations on PA behavioral models. The steps are outlined below.

- To build a MARS mapping function, an ensemble of PA instances are first generated by perturbing the behavioral model parameters. Then a carefully crafted test stimulus is used to obtain a set of envelope responses from these different instances. The

responses are captured using an envelope detector at the output of the PA. The responses are the sampled and fed to the baseband where a mapping between the output responses and the behavioral parameters is generated. If transistor-level ADS simulations are used, a mapping between the parameters (process and bias) and the corresponding output envelope responses can be generated.

- During actual operation of the transmitter, the test same response (stored in the DSP) is used to capture the envelope 'response-features' of the transmitter. The test is applied during transmitter idle time or, alternately, can be incorporated into the training symbol sequence that is normally used for estimating channel conditions in communication systems.
- Using the captured 'response-features', the behavioral performance parameters are estimated, and AM/AM and AM/PM curves are obtained using Equations (29) – (30). The inverse of these curves are then computed and stored in look-up tables (LUT).
- The inverse characteristics stored in AM/AM and AM/PM look-up tables are used to tune the predistorter transfer function.
- Additionally, alternate test framework is used to estimate the 'best' set of adaptive filter coefficients for tuning. The adaptive filter then operates in transmitter baseband to fine-tune for improved performance (linearity).
- The control block coordinates the test response capture, diagnosis, and tuning of the predistorter functionality during the normal operation of the transmitter. Additionally, the control block also strives to operate the PA with high power consumption efficiency. This is done by continuously changing the bias voltage in small steps, diagnosing the PA performance, and tuning the predistorter transfer function as

required within specified bounds. The control loop thus optimizes the PA operation towards higher efficiency.

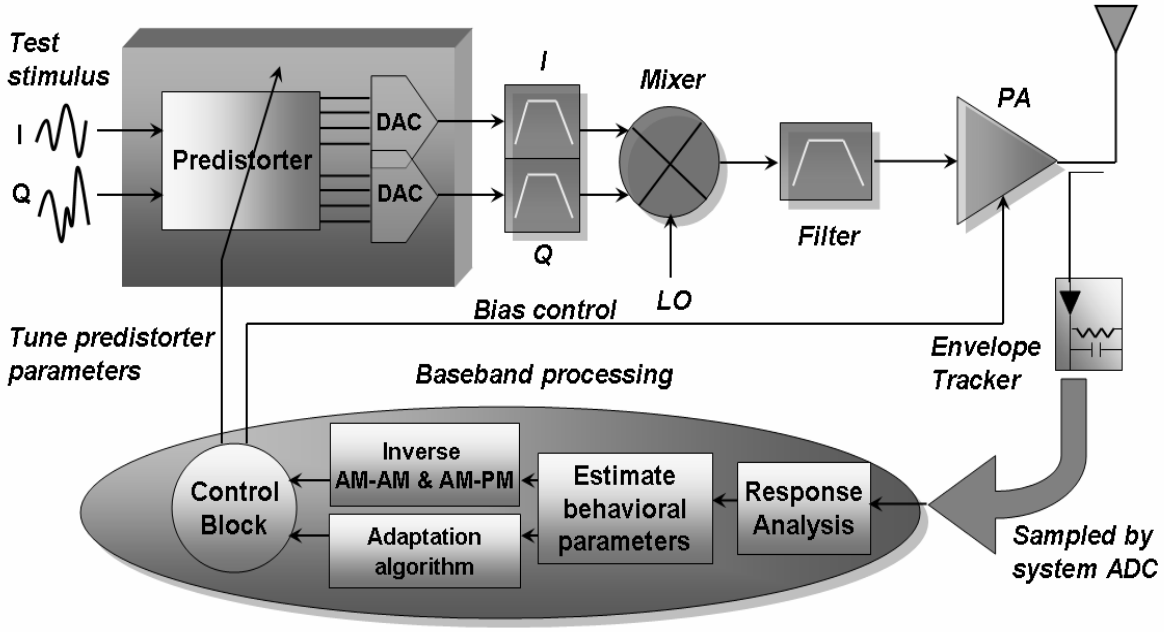


Figure 59 The proposed transmitter diagnostic testing and compensation approach

It is observed (Figure 60) that the amplitude error reduces very gradually (requiring more than 100 iterations for convergence) with arbitrary initial filter coefficients. With the estimated initial filter coefficients, it is observed that there is considerable *convergence speed-up (10X)* as observed in Figure 60. Thus, fine tuning the predistorter can be achieved by using an adaptation algorithm in conjunction with alternate diagnostic testing and compensation.

As seen from the plots, these parameters are predicted with good accuracy. Figure 61 shows the transmitted OFDM-QPSK constellation plots with and without digital predistortion for a single PA instance. As observed from the plots, the non-linear characteristics of the PA (Equations (29) & (30)) are accurately modeled using diagnosed parameters, thereby, improving the transmitted constellation through LUT-

based correction. Before tuning, the transmitted QPSK constellation is cloudy due to the effect of nonlinearity. The use of the above described tuning approach calibrates out the non-linear effect of the transmitter from the constellation.

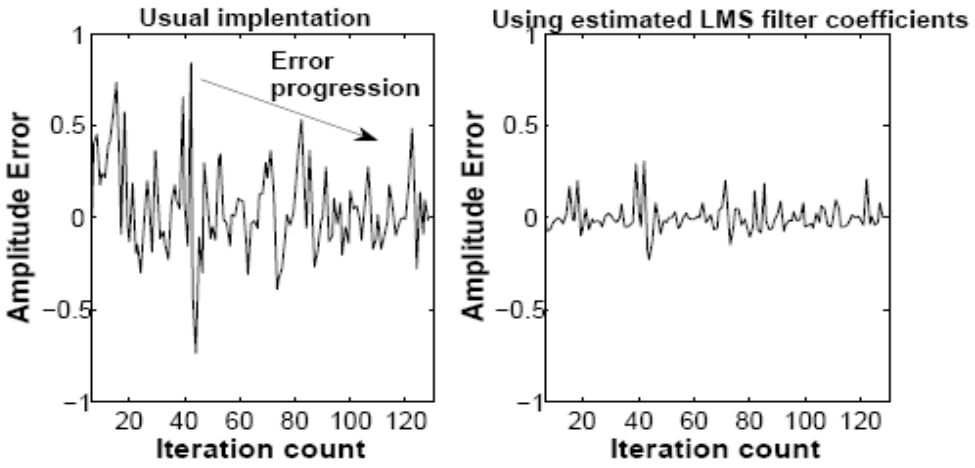


Figure 60 LMS error progression for amplitude tracking

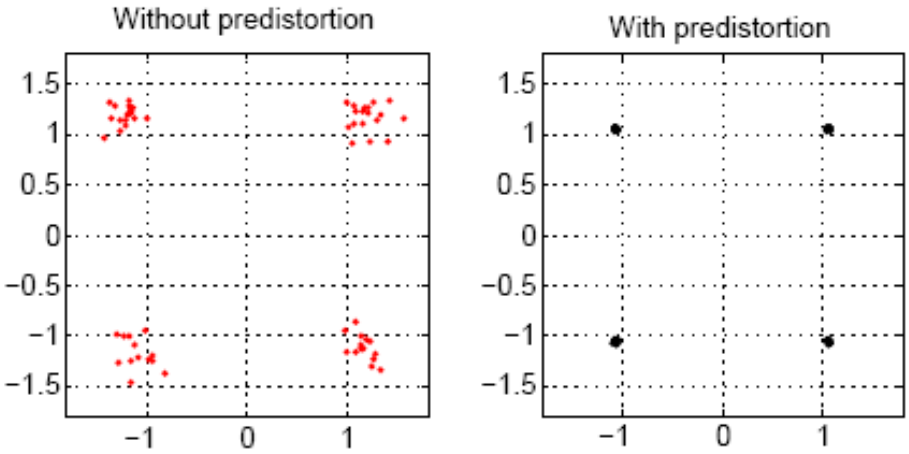


Figure 61 OFDM-QPSK constellation plots for a transmitter

3.2 LOOPBACK TESTING AND TUNING FOR RECEIVER COMPENSATION

Loopback based alternate testing of RF transceivers is a technique where the performance parameters of a complex transceiver is estimated using a simple test approach, where the output of the transmitter is looped back to the receiver to estimate

the system parameters However, non-idealities present in the transmitter result a poor test quality. The use of sensors at the output of the transmitters has been proposed to address this problem and improve the test quality. Though the use of the sensors improves the prediction accuracy of the transmitter specifications, the receiver test quality remains poor due to the non idealities in the transmitter. Due to these non-idealities, the signal at the output of the transmitter is not 'clean'. If a corrupted signal is used as the test stimulus for the receiver, the predicted specifications from the test response turn out to be inaccurate. The transmitter non-idealities also reduce the amount of information available at the receiver baseband for test and diagnosis. In this work, diagnostic testing and tuning of the transmitter is proposed to tune out the effects of non-idealities using the approaches described earlier. This allows a relatively 'pure' signal to looped-back into the receiver for testing purposes.

3.2.1 Loopback Testing

The step by step approach of the proposed loopback-test methodology is described below

- The transmitter is first tested using a test input by observing the sensor response at the output of a transmitter and using alternate test to estimate the transmitter specifications.
- The inverse characteristics of the transmitter are generated from the estimated specifications and this information is used to pre-distort the transmitted signal in the baseband.

- In addition applying inverse transmitter transfer function on the baseband signal, adaptive algorithms like LMS are used to further fine-tune the transmitter to generate a clean signal at the output of the transmitter.
- The tuned output of the transmitter (clean signal) is then used to test the receiver by observing its baseband response using alternate test concept.

Experiments were conducted for the validation of the proposed approach using alternate on a set of 200 transceiver instances. In alternate test, a set of instances are used as a training set to build a regression map between the specifications of the instances to the measured responses of the system to a test input. 150 instances were used here to develop the regression model between the specifications and the measurement responses. The use of a defect filter to screen out catastrophic faulty devices is assumed once gain. 50 instances were then used for validation purposes. The transmitter and receiver gains were used as the specifications of interest. Improvement in the test quality in terms of improved prediction of the gain values of the receiver is used as a proof-of-concept approach to demonstrate the advantages of using tuning while testing. Figure 62 shows the prediction of the transmitter gain for 50 instances of the DUT. Envelope responses (without any tuning) corresponding to each instance of the transmitter was fed to the developed model to predict its gain. The goodness of prediction was demonstrated by the close tracking of the predicted points with the solid line in Figure 62. The obtained transmitter outputs are then looped back to the receiver. Baseband data corresponding to each instance were then used to predict the receiver gain. The prediction plots are shown in Figure 63.

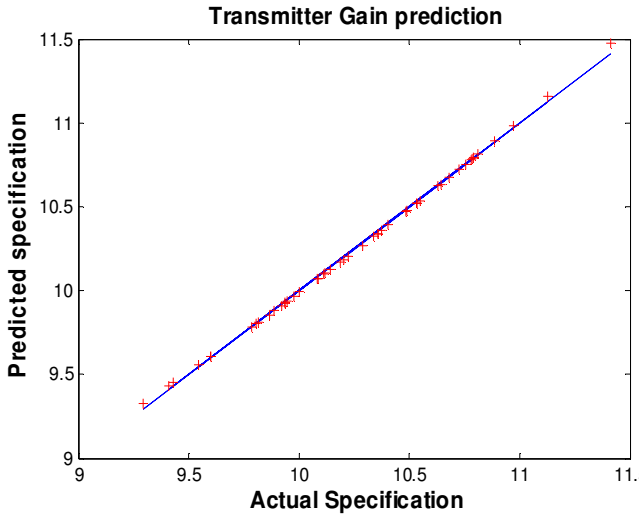


Figure 62 Prediction of transmitter gain

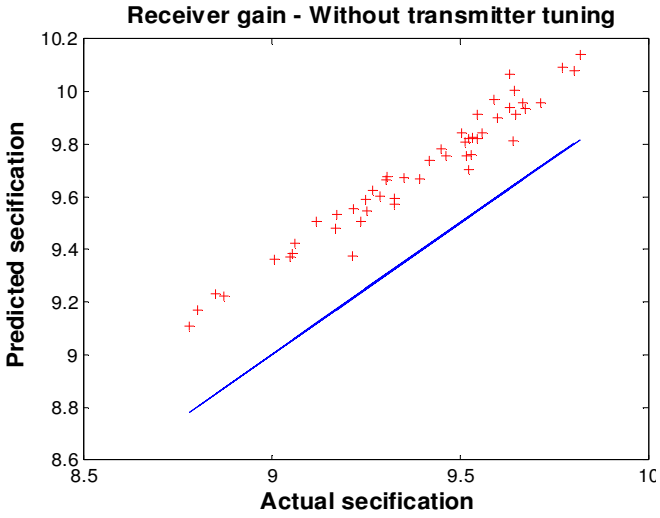


Figure 63 Prediction of receiver gain without tuning

As expected, the presence of variability in the receiver test stimulus (transmitter output) results in a poor prediction for receiver gain. In the proposed approach, each instance of the transmitter is tested for its gain using alternate test based approach. After the testing phase of the transmitter, each instance is tuned for its non-idealities and process variation. The tuned output of each transmitter is looped back to the receiver instances and the subsequent baseband data is used to test for the receiver gain. The

prediction plot for receiver gain using this approach is shown in Figure 64. The plots show a significant increase in the test quality. The improvement in the receiver prediction is quantified in terms of prediction error for both cases in TABLE . The demonstrated results show the significance of tuning the transmitter for enabling loopback testing.

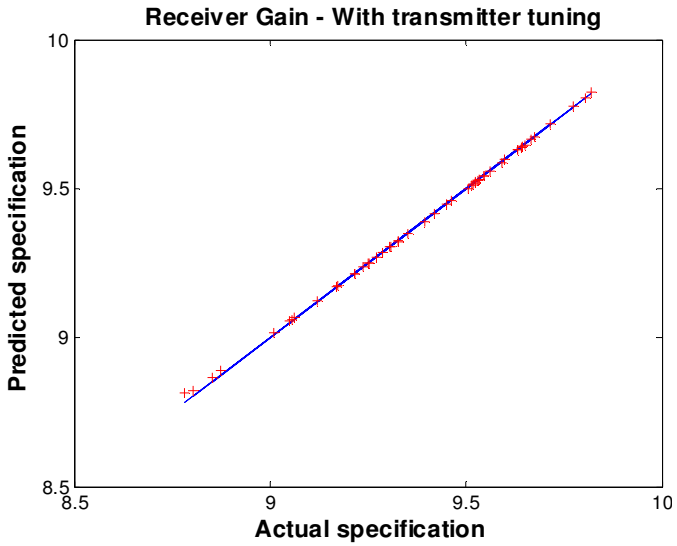


Figure 64 Prediction of receiver gain after tuning

TABLE 8 Improvement in loopback testability after transmitter tuning

Type	Without tuning	With tuning
Relative Prediction error	0.3021	0.0068

3.2.2 Tunable Receiver

The previous section discussed the loopback testing in transceivers. In this section, a loopback test enabled receiver tuning approach is discussed. The key idea is to use loopback testing to dynamically monitor the system performance and perform tuning to maintain the pre-set level of operation under degrading conditions. The receiver is

dynamically tuned to ensure optimum system performance for changing channel conditions (between the transmitter and receiver). The channel between the transmitter and receiver consists of a cable, filter and attenuator. These elements are altered to simulate changing channel conditions. For example, increasing attenuation in the channel reduces the signal strength at the receiver and vice versa. As the received signal strength falls below the threshold, the system performance metrics are not met. Once this occurs, an algorithm running in the DSP starts tuning the LNA to compensate for performance degradation.

The receiver should be designed to be adaptable to enable the dynamic tuning. For study purposes, an LNA is designed here with varactors to enable adaptability. LNA is a key component in a receiver chain and determines the sensitivity of the receiver. Important LNA specifications include gain, NF, and IIP3. The LNA gain specification directly affects the overall sensitivity of the receiver. Maximizing the LNA gain increases the likelihood of detecting weak input signals. NF gives a measure of the amount of noise added by the LNA to the received signal. Increasing NF decreases the SNR of the baseband signal that is fed to the ADC. The NF of the LNA should therefore be kept to a minimum. IIP3 specification is correlated with the non-linearity introduced by the device. LNA design therefore involves tradeoffs between these specifications and the total power consumption.

The varactors serve as tunable capacitive elements in the LNA with control signals from the DSP. Critical reactive elements in the LNA matching network are replaced with a varactor-inductor combination that provides an identical value of reactive impedance. The key specifications of the LNA are sensitive to the values of

these capacitive elements. Thus, adaptability of the LNA can be achieved. The advantage of using varactors for gain control is that it consumes very less power as opposed to using AGC in the baseband. It can be implemented on-chip with very little area overhead. While gain control of the signal using AGC might introduce some non-linearity, enabling tunablity using varactors maintains the linearity of the LNA.

To monitor the performance of the receiver, the power of the received signal at the output of the LNA, an RMS detector is employed. RMS detectors are simple circuits consisting of a forward-biased diode together with some capacitive and resistive elements providing an output DC value. Use of diode-based detectors as sensors has been published extensively in literature. The DC output of the detector provides sufficient information about the output power level. This information can be extracted using a simple ADC. The requirements on the ADC are not stringent - a low sampling rate ADC would suffice. Moreover the resolution requirement of the ADC is not very high. It is therefore a low-cost overhead. Another option would be to use the on-board ADC by time multiplexing with the actual received data. The baseband processor can then track the receiver power level by monitoring the sensor output. If the signal power falls below a threshold, reconfiguration (tuning) is turned on by the baseband processor, and the circuit is tuned to check if improvement is possible.

3.2.2.1 . LNA Design

A single stage common-source LNA with a center frequency of 2.45 GHz (WLAN) is designed for this purpose. The design uses discrete board-level components on FR-4 dielectric and an RF bipolar transistor NESG2021 [136]. The schematic of the designed LNA is shown in Figure 65. As illustrated in the figure, two inductors in the

input and output matching networks are replaced with inductor-varactor combinations. SMV-1408 [137] is chosen as the varactor due to its superior high-frequency performance. As seen in the figure, inductor *L7* (4.8nH) is replaced with a 6nH inductor in series with a varactor. The combination provides an inductance that has a tunable range between 3.5-5.5nH. It is observed that the tuning range of the varactor is frequency-dependent. The design therefore requires recalibration when the frequency of operation is changed.

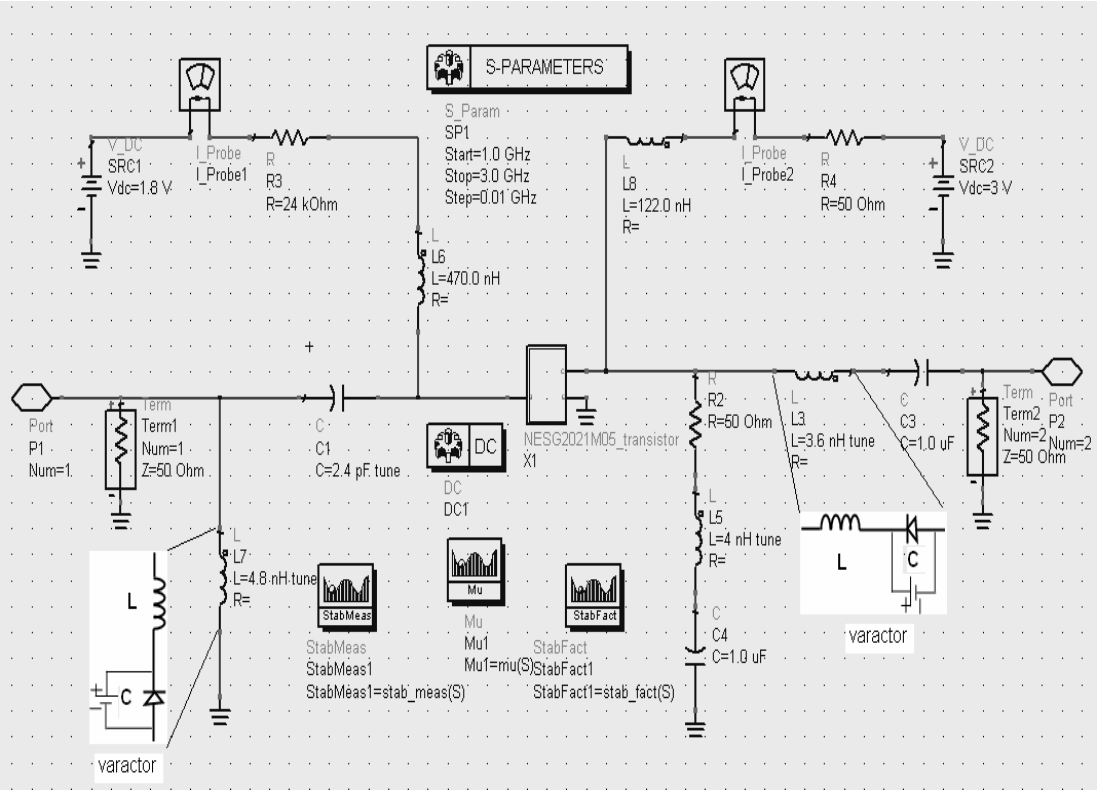


Figure 65 LNA schematic

3.2.2.2 . Sensor Design

An RMS detector that serves as the sensor is also designed and integrated with the LNA on the PCB. The detector shown in Figure 66 is used as a sensor due to its simplicity, low-cost and reduced sensitivity to process parameter variations. A two-diode

configuration is used here as it offers good temperature compensation [138][139] compared to a single diode. The bias and matching networks of the sensor are designed to set the region of operation and to minimize the mismatch the LNA, respectively. The output DC voltage of the detector is proportional to the square of the RF input voltage in the small-signal region of operation i.e. input power in the range of -40dBm to -10dBm. This is the typical range of signal power levels received by a wireless receiver during actual operation. An optimal input matching network for the senor is required to maximize its sensitivity and requires careful design. Simulation and measured results for the output DC voltage of the detector for different power-levels of the input RF signal is shown in Figure 67.

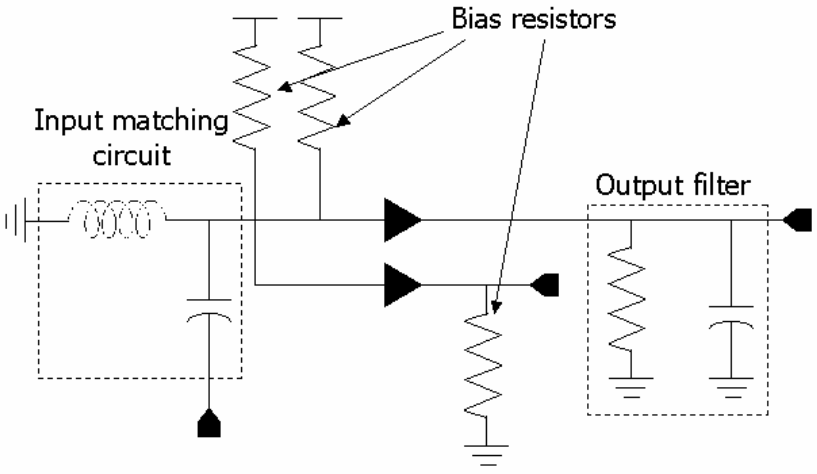


Figure 66. RMS detector schematic.

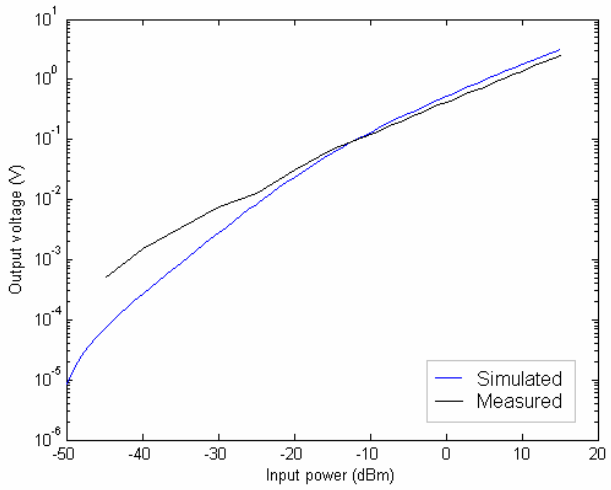


Figure 67. RMS detector performance for varying input power.

3.2.3 Receiver Test

For purposes of study, a complete wireless transmitter is designed and interfaced with the reconfigurable LNA mentioned in the previous section. The RF components of the transmitter that include the band pass filter, mixer and PA are implemented with discrete transistors on FR-4 substrate. The RF section of the transmitter is interfaced to a PC through a National Instruments data acquisition card (DAQ) card [140]. The DAQ card has a maximum sampling rate of 4Msps and simulates the DAC interface in a practical transmitter. The PC serves as a base band DSP processor that transmits data bits to the RF section. An illustration of the setup is given in Figure 68.

A MATLAB code running in the PC performs the following functions. Random binary data is generated initially and the data is then quadrature-QPSK modulated to obtain a sequence of complex numbers. The modulated data is then fed to a 128-point IFFT module that generates a complex time domain waveform. The IFFT output is then transmitted through the DAQ to the RF section. The above mentioned sequence of steps

is similar to the OFDM modulation that is performed in communication systems. In an actual WLAN system several modulation schemes such as BPSK, QPSK, 16-QAM, and 64-QAM are used to provide variable data rates. Due to the bandwidth constraints imposed by the DAQ, the modulation is restricted to QPSK in the current setup. The bandwidth of the baseband data transmitted is set at 1MHz, which is well within the limits of the DAQ card. The base band data is then up-converted by the RF section to 2.45GHz and then transmitted. The output of the transmitter is then looped back to the LNA through a channel. The channel consists of a cable, and an adjustable attenuator. The attenuator settings are changed to simulate varying channel conditions. For example, increasing attenuation in the channel reduces the signal strength at the LNA input and simulates a bad transmission link. Alternately, the power of the signal transmitted to the DAQ card can be varied to mimic changing channel conditions.

First, the LNA is characterized before performing the loop-back measurements. As mentioned earlier the LNA is designed with varactors that allows for adjustment of the gain during field operation. The LNA characterization is performed using signal source, spectrum analyzer and a DC power supply that sets the varactor voltages. Figure 69 plots the LNA output power for an input power level of -45dBm and three different varactor settings. The LNA output power at 2.45 GHz is measured to be approximately -36.8dB on the upper trace. This translates to a gain of about 8.2dB. The corresponding gain values that correspond to the two lower plots are 5dB and -4.85dB. It is observed that the LNA acts an attenuator (negative gain) in the last case. With different varactor settings and repeated measurements, it was found that the LNA gain (positive) can be varied from 0dB to a maximum of about 8.5dB.

Next, the online reconfiguration scheme is tested with the test set-up shown in Figure 68. OFDM-modulated RF signal is sent out through the transmitter. The LNA output power is continuously monitored to ensure if a satisfactory signal power is received. The signal power is tracked continuously by the sensor and the information is used for baseband processing. To do so, the output of the envelope detector is sampled using the DAQ card and sent to the PC. The output of the LNA is also connected to a spectrum analyzer to get a visual display of the reconfiguration process.

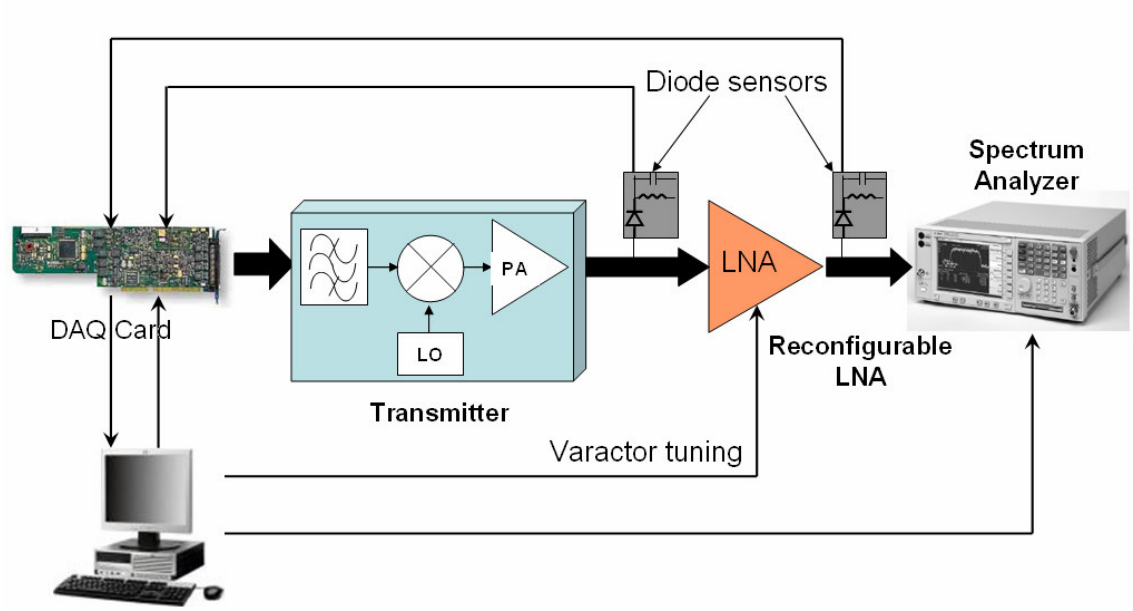


Figure 68. Test set-up for LNA Tuning

With the above mentioned set-up in place, the signal power at the input of the LNA is progressively reduced. As expected, the LNA output power continues to fall until it hits a threshold level. This threshold level is set in the base band controller, and is a measure of the ability of the subsequent blocks in the receiver chain to successfully process the incoming data. It is dependent on a number of factors including system architecture, bit rate, and the type of modulation used. Once it is detected that the received power is below the threshold level (*power threshold*), the reconfiguration loop

is activated. The varactor control signals based on a simple look-up table are used to tune the LNA to achieve power compliance.

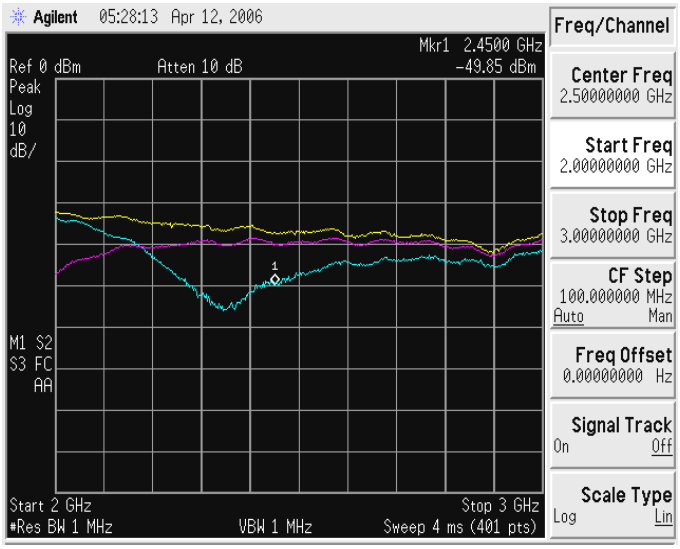


Figure 69. LNA gain for different varactor settings.

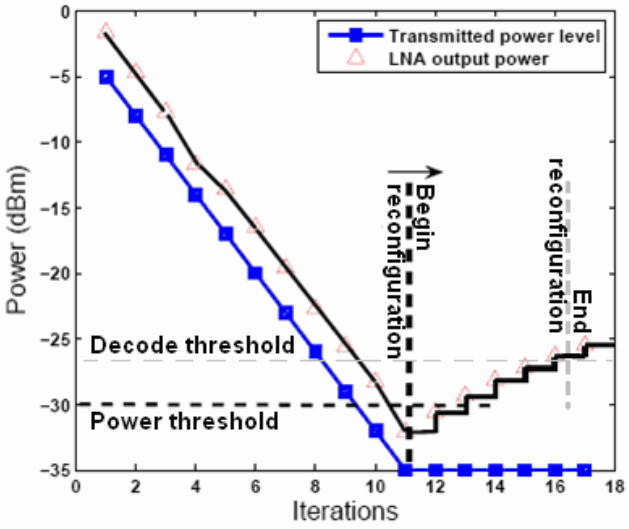


Figure 70. Reconfiguration of the LNA for output power compliance: Measurement response

The response from the measurement is plotted in Figure 70. The transmit power is reduced from an initial value of -5dBm to -35dBm. The LNA output power threshold is set to -30dBm. As seen from the plot, once the LNA output power falls bellow this

value, the PC starts to reconfigure the LNA to bring the output power backup above the threshold. The reconfiguration continues until the 'decode threshold' is reached. This is performed in addition to the baseband control applied in any standard communication system. This method alone may not always be adequate for compensation. For example, if the received signal power is too low or the LNA is already operating with the maximum possible gain, front-end reconfiguration is not adequate. However, this will consume extra power, thereby, reducing the battery life of the device. The objective of the work presented in this section was to demonstrate that using tunable elements like varactors in the RF front-end adds an additional degree of adaptability of a wireless system while using very little overhead in terms of area and power. Moreover, the performance can be dynamically monitored by enabling loopback for test purposes.

3.2.3.1 Loopback Testing and Receiver Compensation

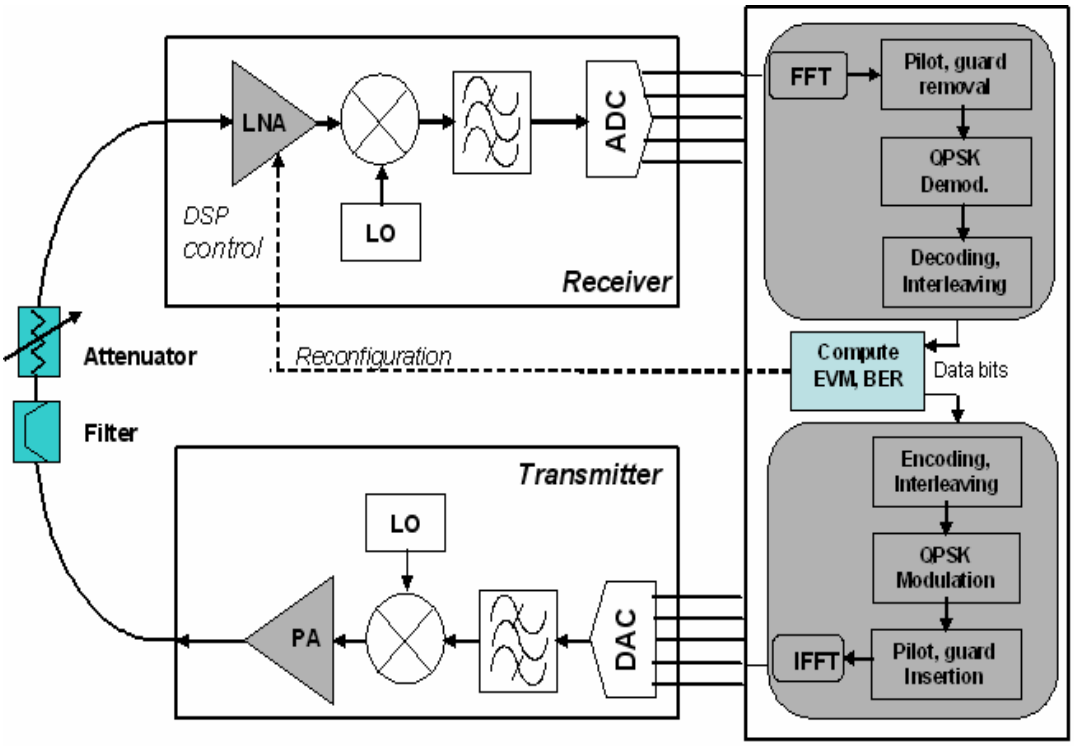


Figure 71 Loop-back test setup for tuning

The loopback hardware test setup is shown in Figure 71. A total of 50 OFDM-modulated data frames transmitted and received by the PC through the RF front-end and DAQ interface. Each frame is a sequence of 256 bits that are QPSK modulated. Initially, with no attenuation in the channel, the transmission is error-free with BER of 0, and an EVM of about 10%. The non-zero value of EVM is due to noise in the circuits, channel and sampling noise of the DAQ card. Next, attenuators (6dB and 9dB) are added to the channel and quality of data transmission is tested. For increasing attenuation values, it is observed that the transmission deteriorates (non-zero BER). There is also a significant increase in the EVM of the received frames. Following this, the tuning option is enabled in the LNA to adapt to the deteriorating channel conditions. The tuning is performed by changing the varactor voltages using control signals from the DSP. The passing condition for successful transmission here was set to BER of zero and an EVM less than 30%. The results are summarized in the table below. For a channel attenuation of 6dB, the optimum varactor voltage after tuning is 6V while for 9dB attenuation, the optimum varactor voltage for successful transmission is 1V.

TABLE 9 OFDM System Specifications

	EVM(%)	**BER**	**Frame error Rate (%)**
Channel Attenuation			
0 dB	10	0	0
6 dB			
Before tuning	>100	0.4	60
After tuning	25	0	0
9 dB			
Before tuning	>100	0.5	100
After tuning	27	0	0

It is observed from the table that the tunable OFDM front-end adapts successfully to changing channel conditions through online monitoring of the data in the baseband

processor. In conclusion, enabling techniques for dynamically adaptive wireless OFDM receiver front-end were described along with simulation results and hardware measurements. Adaptability has direct implications for increased operational reliability of wireless systems. It also enables the dynamic operation of the system with reduced power consumption. The proposed approach can be applied to any wireless transceiver with little hardware or software overhead.

3.3 APPLICATION TO ULTRA WIDE BAND SYSTEMS

In this section, a built-in test and reconfiguration approach for UWB transmitters is presented. The wide operating bandwidth of UWB devices increases the sensitivity of the specifications to process variations, especially at edge frequencies. It is very important to estimate the circuit/system specifications at process corners, and provide compensation at an earlier stage in the design process. The wide bandwidth associated with UWB systems causes the implementation of built-in test and tuning techniques more complicated than for traditional wireless systems. The gain flatness (gain variation over the bandwidth) is one of the most important specifications in UWB systems. It has been shown in the past [141] that small variations in RF gain over the operating bandwidth significantly deteriorate the system-level specifications and the performance. In the proposed method, a test scheme that monitors the RF front-end for gain flatness is presented. If a variation in gain is detected, the circuit is tuned to restore flatness of the gain profile. The tuning also helps in increasing the yield of the devices. The proposed approach shows a significant promise of lowering the overall manufacturing cost of UWB devices.

Common circuit-level specifications for the RF front end in wireless receivers include gain, NF, 1-dB compression point P1dB and IIP3. Due to the low power operation and wide bandwidth of UWB systems, non-linear specifications such as P1dB and IIP3 are not relevant. The system-level metrics include EVM and BER. The system-level specifications of the receiver are strongly correlated with RF front-end circuit specifications, especially the LNA. The following section describes BIT approach for the LNA using sensors, and the tuning technique to meet the system-level specifications under physical and temporal deviations.

3.3.1 UWB Receiver

The design choices for the LNA and bandpass filter are studied first along with their effect of system performance. The antenna, bandpass filter and LNA followed by a mixer comprise the UWB receiver front-end used for study. A description of the antenna model and free-space transmission effects is also presented along with modeling equations.

3.3.1.1 LNA and Filter Designs

LNA is a critical component in the receiver since it determines the noise and signal properties of the entire chain. CMOS-based wideband amplifier topologies reported in literature include cascade [42], resistive-shunt feedback amplifiers [145] and distributed amplifiers. While distributed amplifiers have a wide bandwidth, they are plagued by high power consumption and occupy a large die area. This makes them unfit for UWB implementation.

For the purpose of a comparative study, two different LNAs based on cascade architecture and shunt-feedback technique respectively, were designed. In the cascade LNA, two amplifier stages that are optimized to different frequency ranges are cascaded such that the combined circuit operates over a larger bandwidth. In our design, two common-source (source-degenerated) amplifiers centered at 3GHz and 4GHz respectively, were cascaded to form an LNA with sufficient bandwidth to operate in the first band group of UWB (Figure 72). The input and output of the individual stages are closely matched to 50Ω to avoid any mismatches between the stages. Figure 73 shows the plots of LNA gain and noise figure. It is seen that the gain (S21) is about 15dB and a NF less than 3dB in the frequency range of interest (3-5 GHz).

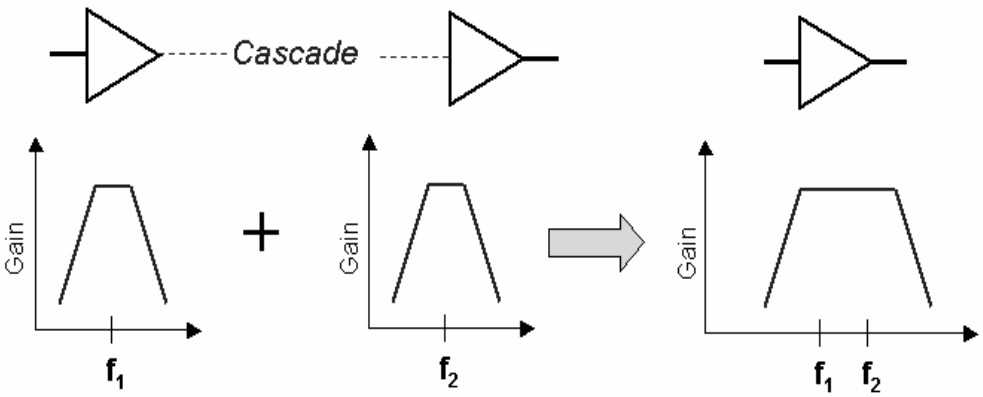


Figure 72 Wideband LNA design using cascade architecture

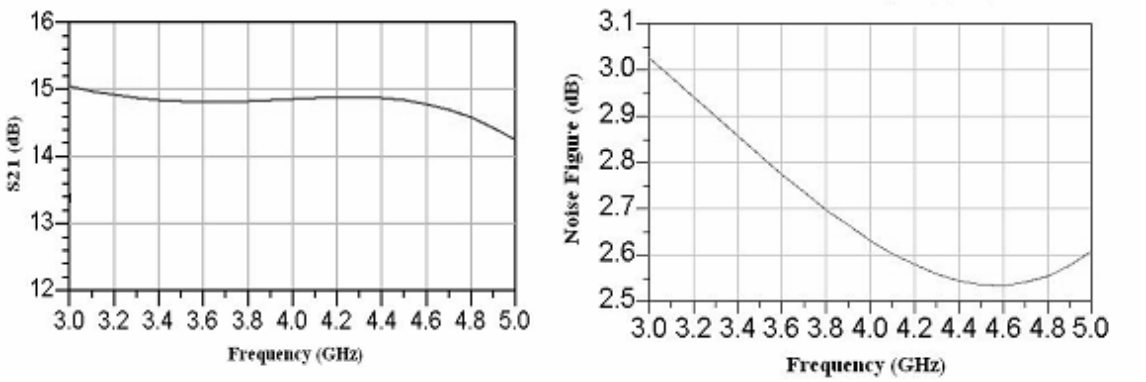


Figure 73 Cascade LNA Characteristics

Resistive-shunt feedback amplifiers are known to provide a wide bandwidth and flat gain. A shunt-feedback LNA with a peaking inductor at the output was designed here. While the shunt-feedback resistor sets the bandwidth of the amplifier, it also affects the noise figure of the LNA. The value of the feedback resistor was optimized in the design to achieve the required bandwidth while maintaining a sufficiently low noise figure. Figure 6 shows the plots of S21 and NF of the shunt-feedback LNA. The gain is over 11dB and NF lesser than 3dB in the UWB frequency range.

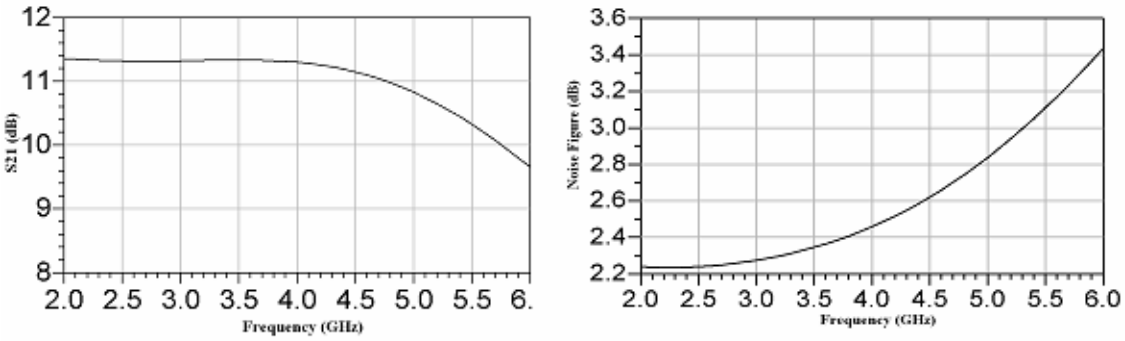


Figure 74 Shunt-feedback LNA characteristics

Bandpass filters in the front-end play a crucial role in limiting out-of-band energy that might saturate the receiver. Two distributed chebyshev bandpass filters with 0.5dB and 3dB passband ripple respectively, were designed on duroid ($\varepsilon_{r=}$10.2, h = 62 mils).

While the 3dB ripple filter has a higher passband variation, it exhibits sharper stopband attenuation compared to the 0.5 dB ripple filter. This is advantageous in limiting the 802.11a WLAN (5.125-5.25GHz, 5.725-5.825 GHz) signals by providing higher attenuation. The designed 3dB ripple filer attenuates the 5.725GHz signal by approximately 8 dB more than the 0.5 dB ripple filter. The plots for return and insertion loss for both the filters are given in Figure 75 and Figure 76.

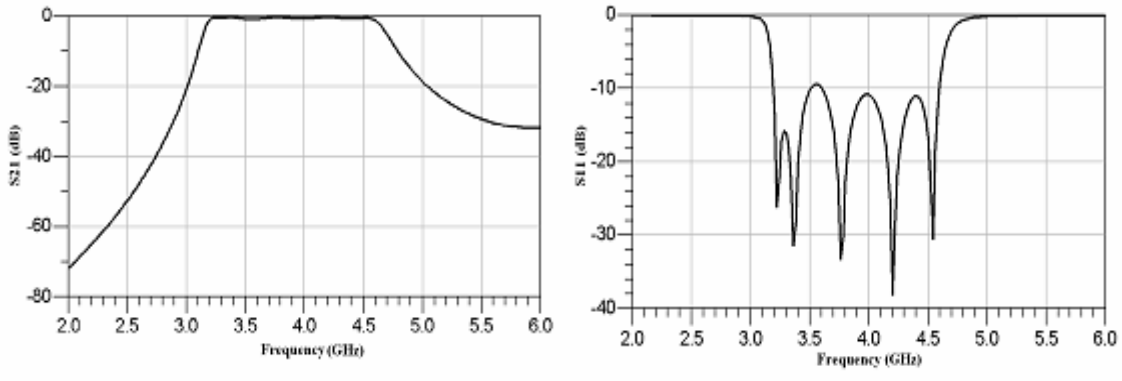


Figure 75 0.5dB ripple filter characteristics

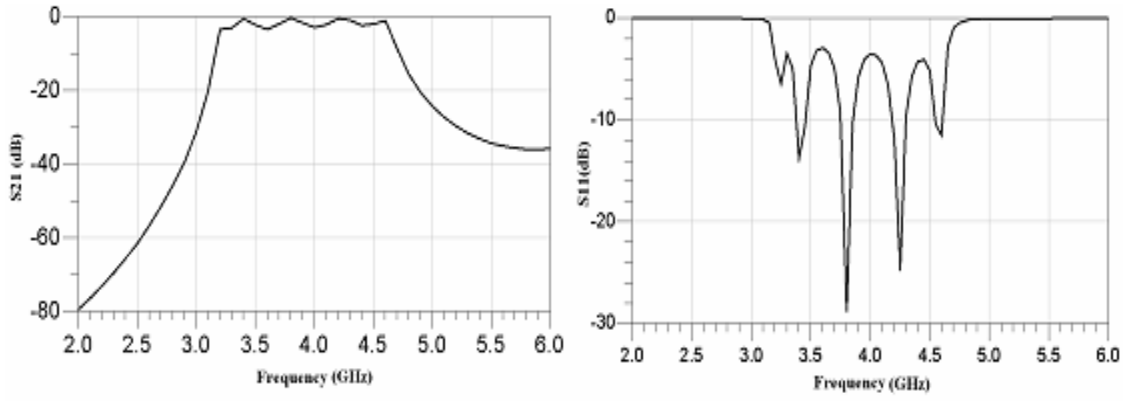


Figure 76 3dB ripple filter characteristics

3.3.1.2 Antenna and Channel effects

The bandwidth of the UWB system makes the antenna design more complex compared a narrow-band system as the antenna parameters vary considerably over the

frequency. Innovative design techniques have been proposed to design low-signature high-performance antennas for UWB systems [142]-[144]]. The design of a 3-6GHz bandwidth omni-directional antenna is presented in [143]. The return loss of the antenna has been shown in Figure 77. While the return loss is low in the frequency band, there is considerable variation in the magnitude (~25 dB) over the band. This variation is typical for wide band antennas and can be very critical in the performance of the systems. For simplicity, an efficiency of 100% is assumed for the antenna, and the return loss data is used to model the antenna.

Estimation of path-loss is another important consideration in wireless system design. The power falls off as the square of the distance as radio wave propagates in free space due to the spreading of the waves. The path loss (L) can be calculated by:

$$L = 20 \log 10\left(4\pi D / \lambda\right) \qquad (42)$$

where, D is the distance between the receiver and the transmitter and λ is the free space wavelength. Figure 77 plots the variation of path loss over frequency.

The above equation suggests that the loss has a frequency-dependence. This is of particular importance in UWB systems due to the wide bandwidth of operation. For example, as shown in Figure 77, the loss L for a 3GHz signal can differ from that for a 5GHz signal by as much as 4 dB. Thus, there is a significant variation of the received power over the frequency band, and the receiver design should compensate for this variation.

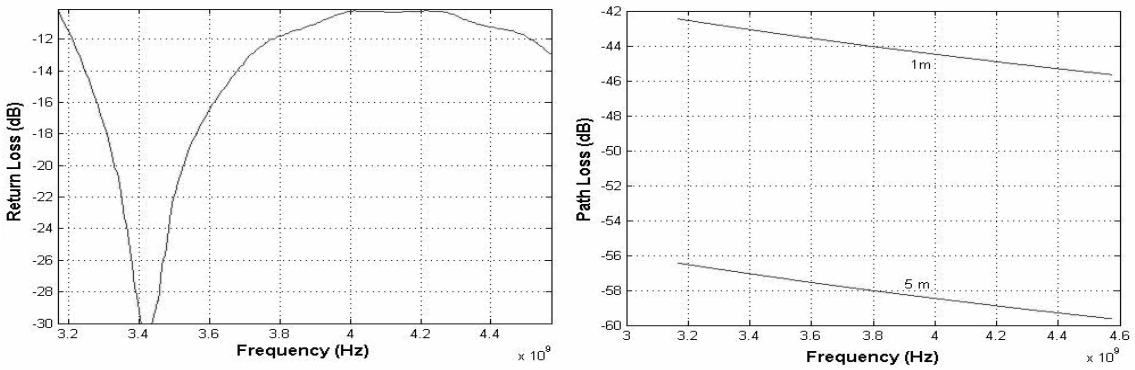


Figure 77 Antenna return loss and path loss

3.3.2 Sensitivity of System Metrics to Design Variations

The test setup simulates the designed UWB receiver system to determine the variation in specification values under process perturbations. The designed system operates from 3.1GHz to 4.8 GHz. Apart from considering process variations, phase noise of the oscillators, non-linearities of the data converters (DAC and ADC) and overall system noise was also considered during the Monte Carlo simulations. A simulation output for EVM constellation is shown in Figure 78. EVM and BER was calculated for the system based on definition given in Chapter 2.

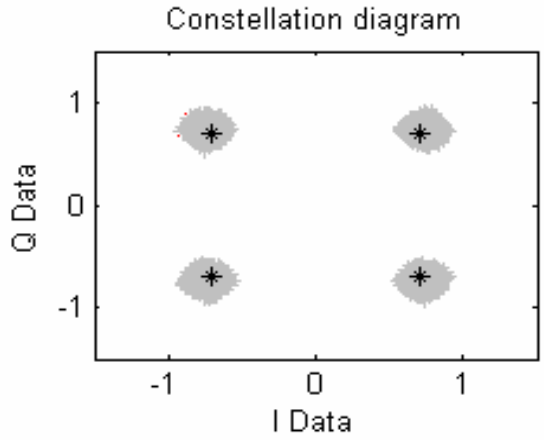


Figure 78 EVM Constellation Diagram

First, the system comprising the 0.5dB ripple filter and cascade LNA in the front-

end was simulated without considering the normal process variations to determine the variations in specifications. Figure 79 shows the distribution of EVM for 100 devices (BER for all the devices considered was 0). The mean EVM value is 8.6% with standard deviation of 0.84%. Next, design variations were considered. Here, the system was simulated first with the cascade LNA and the 0.5dB ripple filter following which, the cascade LNA was replaced by the shunt-feedback LNA. The mean EVM changed to 21.45%, with a standard deviation of 5.09% (Figure 80) for the first case, and 30.45% with a standard deviation of 4.42% for the second case. It was however noted that the BER remained at zero for both the implementations. The EVM is higher when shunt-feedback LNA is used due to the lower gain of the amplifier. In actual implementation, an automatic gain control unit (AGC) in the receiver chain would compensate for this gain variation keeping the EVM within bounds. The results for shunt feedback LNA and 0.5dB ripple filter are shown in Figure 81.

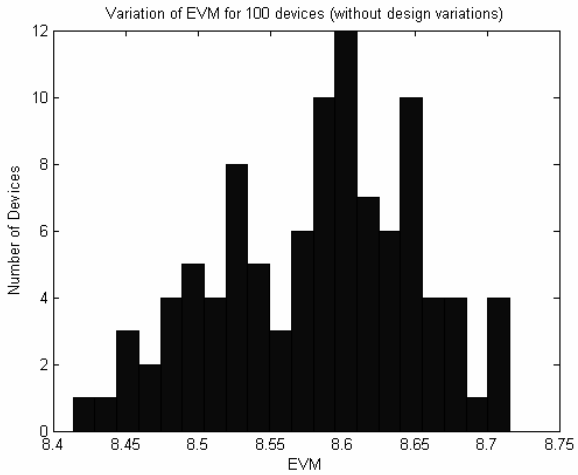


Figure 79 Variation of EVM without design variations (0.5dB filter and cascade LNA)

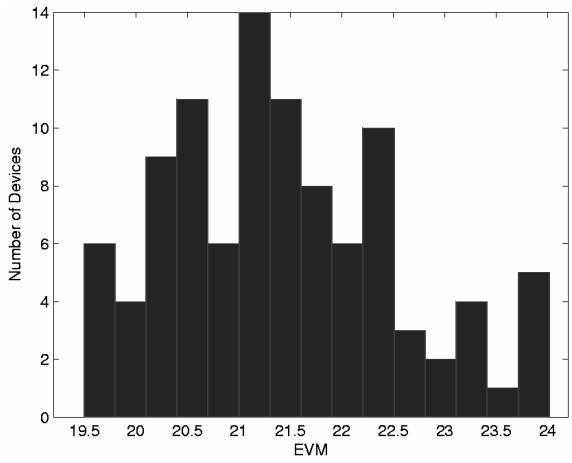


Figure 80 Variation of EVM with design variations (0.5dB filter and cascade LNA)

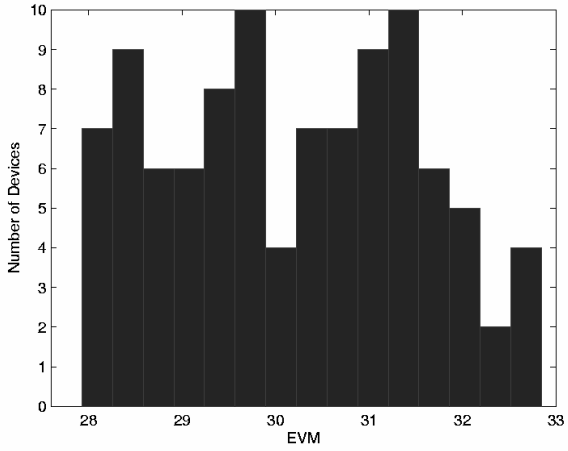


Figure 81 Variation of EVM with design variations (0.5 dB ripple filter and shunt-feedback LNA)

3.3.3 Interference Effects

The system was then simulated for interference tolerance. The interfering signal was an IEEE 802.11a signal at 5.725GHz. The signal power was –15dBm. The simulation results with design variations are shown for the two designs described in the previous section excluding design variations. The simulation results for the 0.5dB ripple filter and cascade LNA are: EVM of 22.3275% with standard deviation of 0.2775%.

It was noted that BER was no longer zero, but increased to 5.6 $X10^{-3}$, with

standard deviation 6.65%. Figure 82 shows the variation of EVM and BER for 50 devices simulated in presence of oscillator phase noise, digitizer nonlinearity, system noise and the interfering signal.

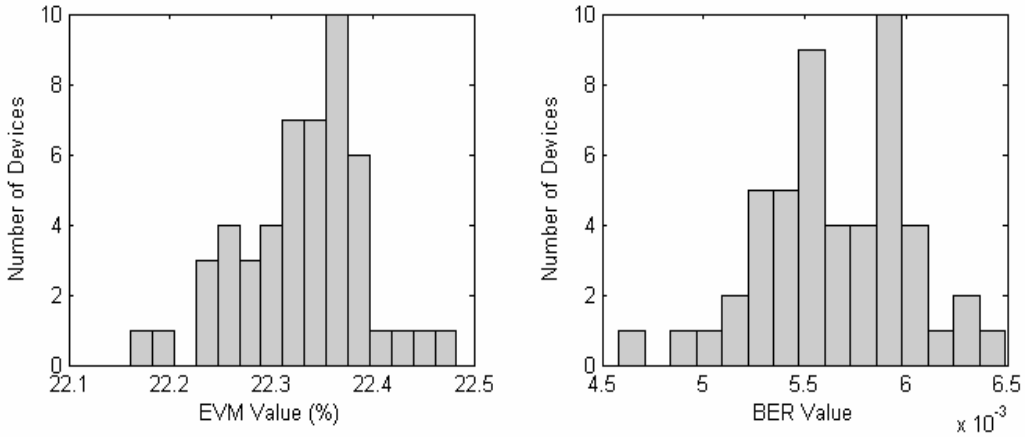


Figure 82 Variations in EVM and BER without design variations

Under process variations, the system was simulated for EVM and BER for the two designs. The resulting mean EVM was 28.83% with a standard deviation of 2.62% for the first case, and 35.22% with a standard deviation of 2.88% for the second. Figure 83 and Figure 84 show the variations in EVM and BER with design variations for the two cases, respectively. The following table (Table) summarizes the performance metrics for the UWB device (0.5dB filter and cascade LNA).

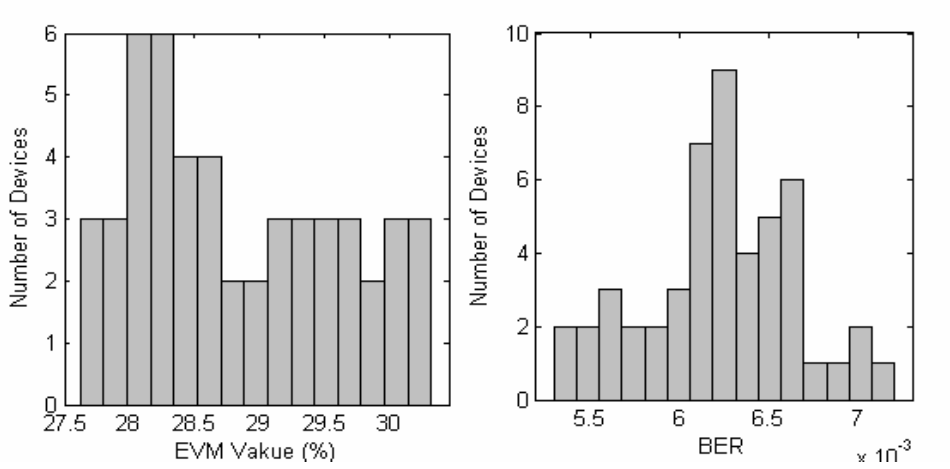


Figure 83 Variations in EVM and BER with design variations (0.5dB ripple filter and cascade LNA)

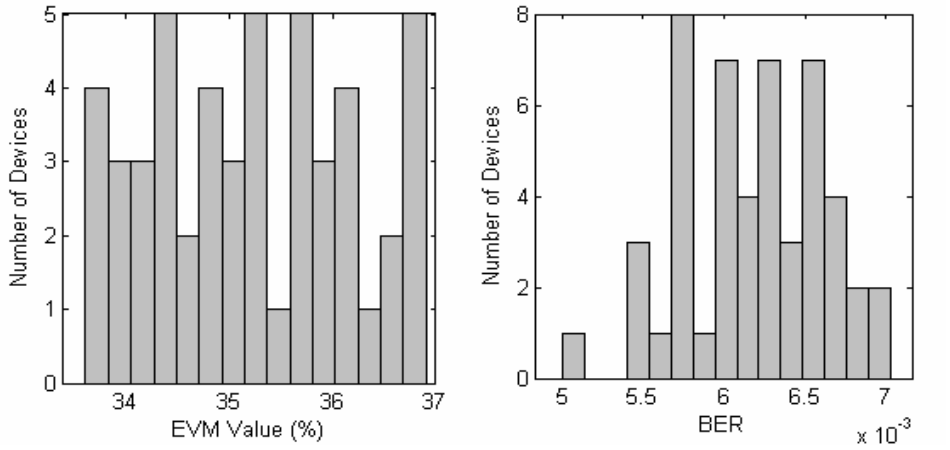


Figure 84 Variations in EVM and BER with design variation (0.5dB filter with shunt-feedback LNA)

Table 10 Comparison of system performances

	Without Interference		**With Interferer (-15dBm)**	
	EVM	**BER**	**EVM**	**BER**
Without Design Variations	μ: 8.6 σ: 0.84%	0	μ: 22.32 σ: 0.27%	μ: $5.6X10^{-3}$ σ: 6.65%
With Design Variations	μ: 21.42 σ: 5.09%	0	μ: 28.83 σ: 2.6%	μ: $6.8X10^{-3}$ σ: 7.022%

As evident from Table , design variations affect EVM considerably. BER, on the other hand, is more robust to variations in performance parameters and is affected to a lesser extent compared to EVM. Thus, during design compensation, designers need to carefully consider EVM to ensure proper functionality of the system. With increasing power levels of interference, it is found that the BER performance of the system is better with the 3 dB ripple filter when compared with 0.5 dB ripple filter. This is attributed to the higher attenuation of the interferer by the 3dB filter. The results for BER simulation are summarized in Table below. The results indicate the trade-off between the passband ripple and interference tolerance needs to given proper consideration while designing the filter for receiver. Simulations are performed on a MB-OFDM UWB system to estimate the effect of process parameter variations on system specifications, viz. EVM and BER. It is observed that there is significant degradation in these specifications due to variations in process parameters. These are further affected if effects of oscillator phase noise, ADC and DAC non-linearities and inherent system noise are considered. It is therefore necessary to get a good estimate of the sensitivity of the system specifications to different designs and correct them through proper compensation techniques at an early stage in the design process.

Table 11 Comparison of BER for the two filters and interference power levels

Interference Power (dBm)	**0.5dB filter, Cascade LNA**	**3dB filter, Cascade LNA**
No Interference	0	0
-15	6.84×10^{-3}	6.98×10^{-3}
-5	8.81×10^{-3}	8.92×10^{-3}
0	1.55×10^{-3}	1.55×10^{-3}
5	3.90×10^{-3}	3.45×10^{-3}
10	7.76×10^{-2}	6.85×10^{-2}

3.3.4 Tunable Receiver

In a UWB receiver, the LNA performs initial amplification of the signal and is the most critical component in the RF front-end that affects the performance of the entire receiver chain. Although various compensation techniques like AGC etc. are employed in transceiver systems to ensure optimal performance, overall receiver operation is still largely affected due to variations in the RF front-end, especially the LNA. Ensuring the correct operation of the LNA therefore, remains critical to the proper functioning of the UWB receiver.

A compensation scheme for the LNA based on continuous self-testing and reconfiguration of the same is presented here. Figure 85 illustrates the overall concept. For error-free operation of the receiver, gain flatness of the LNA is a key specification of interest. The transmitter interleaves and transmits the data between different sub-bands of the UWB spectrum, and the receiver collects RF energy into different sub-bands at different time periods. To monitor the gain of the LNA over various frequencies, a sensor array is embedded into the design, tuned to various frequencies within the range of operation. Sensors at the input and output of the LNA capture the RF signal to evaluate the gain at various frequencies. Alternately, sensors can also be inserted at the mixer output. The sensor outputs are then sampled and the information is processed by the DSP for reconfiguration. The LNA is designed with tunable elements allowing for calibration, with control signals from the DSP. If the gain profile is not flat, the embedded sensors detect this variation. Based on the information from the sensor array, reconfiguration of the LNA is performed to compensate for variation in gain flatness.

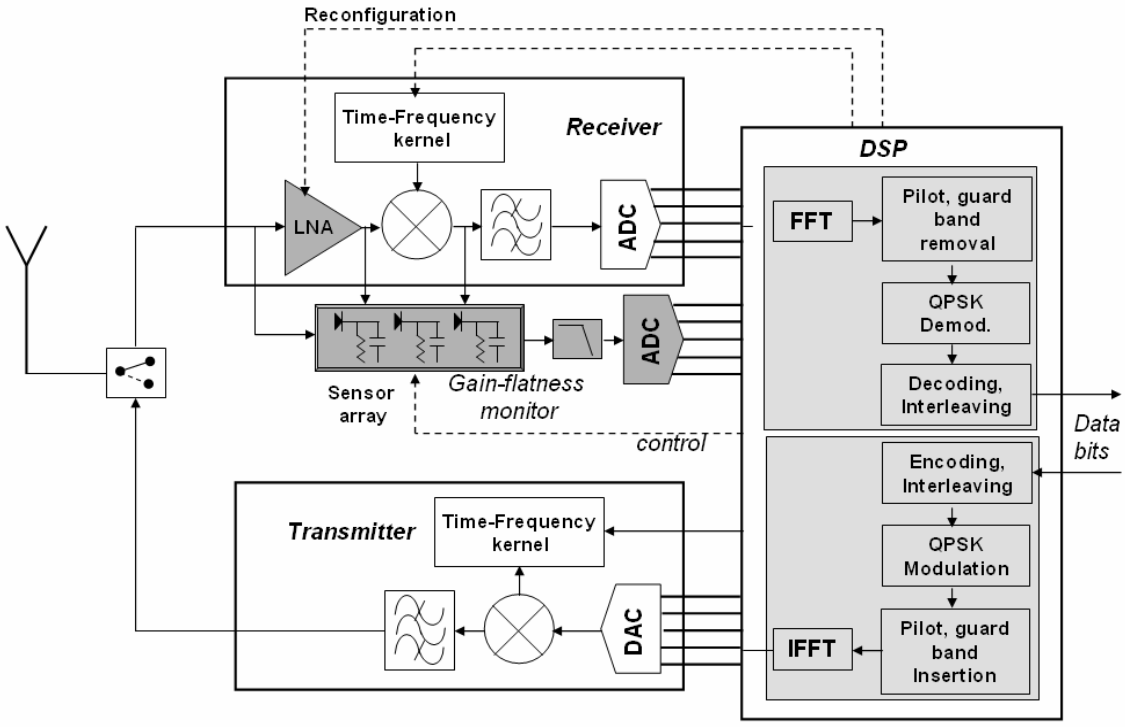


Figure 85 BIT and reconfiguration scheme for UWB transceiver

In this scheme, the band-hopping scheme of MB-OFDM is used for evaluating the gain flatness of the LNA. It is critical for the reconfiguration scheme to consist of simple low-cost elements that do not increase the area overhead, and cost of the UWB device. As seen in Figure 85, the additional components include the sensors (with matching networks), tunable elements in the LNA, low-pass filters and an ADC. The requirements on the ADC are not stringent as the input signal is DC. A 4-bit low sampling speed ADC with a 10mV resolution would suffice. The sensor is chosen to be simple with a minimum number of elements. The LNA and sensor designs are described in the following sections.

In the past, several wide-band LNA topologies such as shunt-feedback, cascade, and distributed LNA have been reported in literature. A shunt-feedback LNA with a peaking inductor at the output is designed for this work. Resistive-shunt feedback

amplifiers provide a wide bandwidth and flat gain. While the shunt-feedback resistor sets the bandwidth of the amplifier, it also affects the noise figure of the LNA. The feedback resistor is therefore a critical component, and is a good choice for the tunable element in the LNA. Moreover, due to the wide-band operation of the LNA, the use of reactive elements for reconfiguration without affecting the gain flatness is not possible. Figure 86 shows the schematic of the LNA with the tunable shunt feedback resistors that are used for tuning.

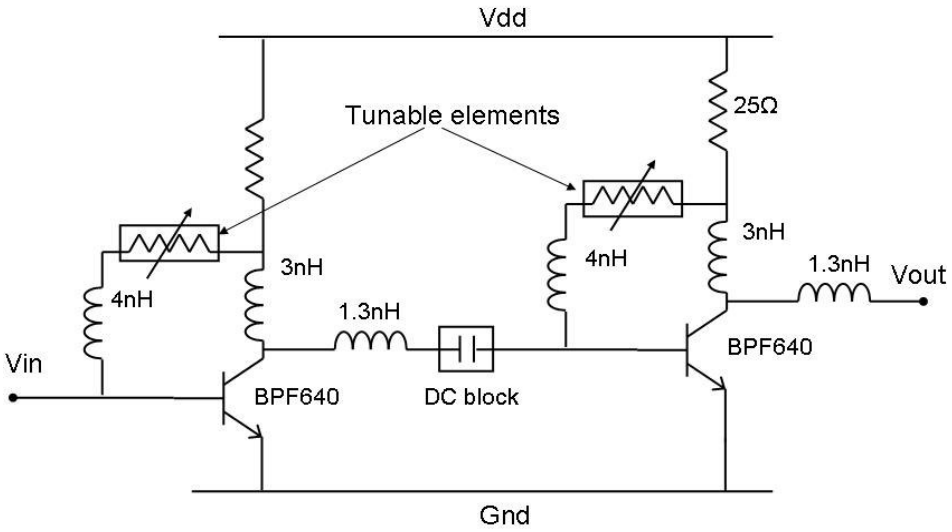


Figure 86 LNA schematic with tunable shunt feedback resistor

The nominal value of the feedback resistor was optimized in the design to achieve the required bandwidth while maintaining a sufficiently low noise figure. The LNA consists of two identical stages which are cascaded together. The transistor used in the design is BPF640 from Infineon technologies due to its good high frequency performance. Figure 87 shows the plots (solid line) of S21 and NF of the LNA. The gain is over 20dB and NF lesser than 3dB in the first band group frequencies (3-5GHz).

3.3.4.1 Wideband Sensor

A simple diode-based detector shown in Figure 88 is used as a sensor due to its simplicity, low-cost, and reduced sensitivity to process parameter variations. As explained earlier, the output DC voltage of the detector is proportional to the square of the RF input voltage in the small-signal region of operation i.e. input power in the range of -50dBm to -10dBm. This is well suited for UWB devices with the low received power levels. A two-diode configuration is used once again as it offers good temperature and process variation compensation. An optimal input matching network is required to maximize the sensitivity, and therefore needs to be tuned for the three different frequency bands.

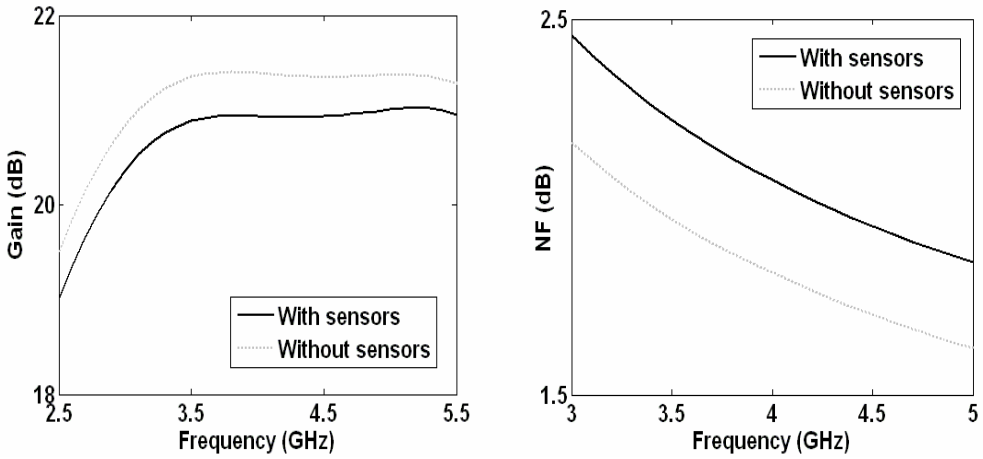


Figure 87 Comparison of LNA gain and noise figure with and without sensor

This is easily achieved by switching the inductor *L1*. The output DC voltage of the detector for different power-levels of the input RF signal is shown in inset of Figure 88. The sensor bias and matching network are designed to minimize the mismatch between the LNA and the sensor. The performance of the LNA with the sensors added (dashed line) is compared with its actual operation in Figure 87. Inclusion of sensors has

a minimal effect on gain flatness and NF of the LNA. As expected, there is a slight reduction in gain due to the sharing of output power to the sensor, and an increase in NF due to the addition of sensor bias resistors.

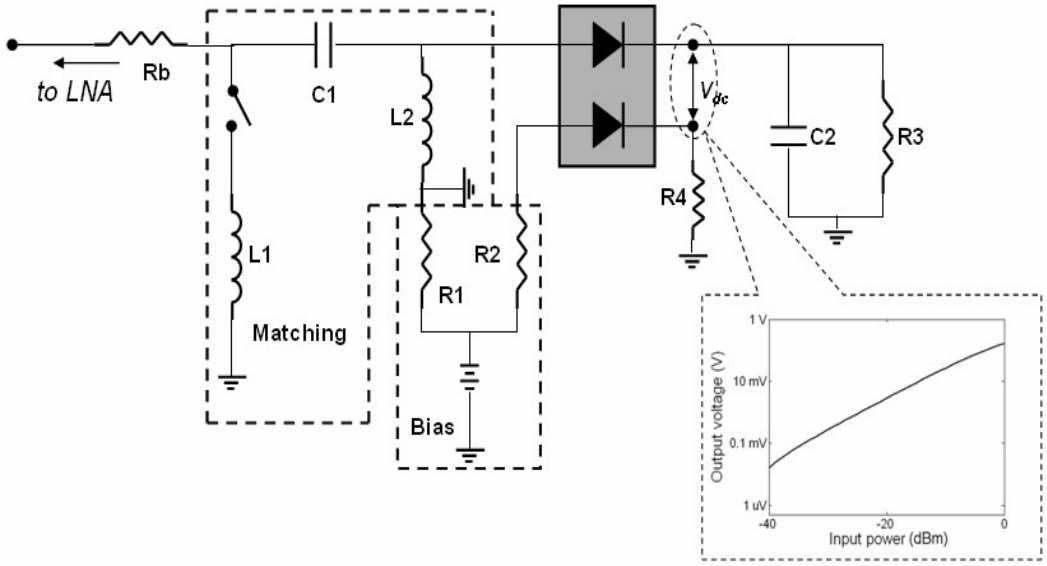


Figure 88 LNA Sensor with output

3.3.4.2 Simulation Results

Monte-Carlo simulations were performed on the LNA to perturb process parameters. Figure 89 shows the gain of a specific instance of the LNA (dashed line) and the corresponding base band constellation. A MATLAB code is used to mimic the MB-OFDM baseband functionality. The quality of the received data can be studied my monitoring the received constellation. From Figure 89, it can be seen that the gain is not flat over the frequency range due to the perturbed parameters. Also shown in Figure 90 is the decoded constellation at the receiver base band. The constellation is scattered (EVM of 38.73%), thereby, indicating imperfect operation of the receiver. With the tuning circuit present, this gain variation is detected by the sensors, and the LNA is tuned

to reduce this variation. The gain of the tuned LNA is shown as the solid line in the figure, and an improved constellation (EVM of 25.92%) is obtained after compensation.

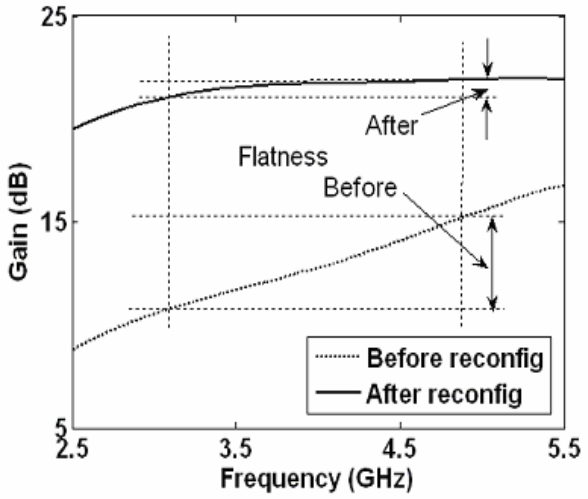


Figure 89 Gain of LNA Instance 1 and reconfigured LNA

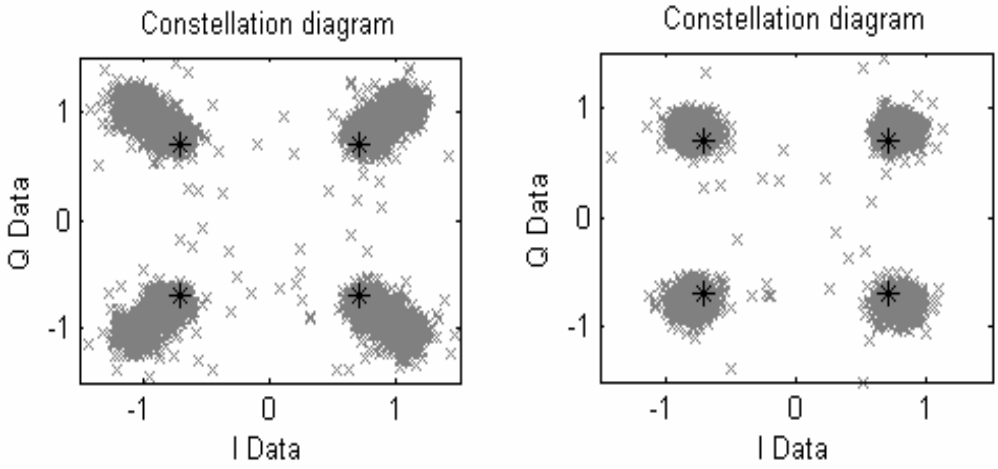


Figure 90 EVM plots for LNA instance 1 and reconfigured LNA

Table gives the specifications of two different process perturbed LNAs and their corrected versions, respectively. The correction was performed by tuning the shunt-feedback resistor in the LNA. It can be seen that there is a considerable improvement in performance for the reconfigured LNA. The variation in sensor outputs over the frequency range is reduced, and the baseband constellation is less scattered. The

transceiver chain was also simulated for BER in the presence of channel noise, LO phase noise and ADC/DAC system non-linearities. Again, the performance of the reconfigured instances is observed to be better. The above mentioned scheme is simple and effective in providing an enhanced quality of service (QoS) in terms of received erroneous bits. This also has a direct effect of increasing the yield of the device. Moreover, this simple sensor-based self-test approach can be used to reduce test time in a production test environment.

Table 12 Receiver specifications with reconfiguration

	Instance # 1	**After Correction**	**Instance # 2**	**After Correction**
Gain				
Mean	12.62dB	19.56 dB	12.53dB	21.58 dB
Minimum	11.3dB	19.44 dB	10.55dB	20.89 dB
Maximum	14.35dB	19.74 dB	14.67dB	21.85 dB
Sensor O/p				
Band 1	15 mV	86 mV	14 mV	85 mV
Band 2	32 mV	105 mV	30 mV	110 mV
Band 3	42 mV	126 mV	35 mV	123 mV
EVM	38.73%	25.92%	40.47%	25.84%
BER	6.1×10^{-3}	6.72×10^{-3}	6.0×10^{-3}	6.37×10^{-3}

3.4 BIT APPROACH FOR FREQUENCY MODULATED TRANSCEIVERS

Phase and frequency modulation schemes are used in many important communication and wireless applications. A key defining characteristic of phase/frequency modulated systems is the constant amplitude of the transmitted signal making it impossible to use envelope-based BIT techniques. Phase and frequency modulation techniques are an integral part of several wireless communications systems including GPS, radio frequency identification systems (RFID), Bluetooth, and public

communications services (PCS) systems etc. [146]-[149]. The use of frequency/phase shift keying (FSK/PSK) for spread-spectrum frequency transceivers has been proposed and future multi-mode, multi-standard radio communications are expected to include phase/frequency modulations.

Envelope detector based test techniques described in the previous sections is not applicable to phase/frequency modulated devices due to their constant amplitude envelopes. It is more appropriate to use peak and RMS sensors for this purpose. But the peak and RMS sensors proposed in literature are either complicated or do not work well for constant amplitude signals. Moreover, these sensors are very sensitive to process variations and test quality is affected due to non-idealities in the sensor.

To address the issue of built-in testing of frequency modulated systems, an efficient technique is presented in this section that uses a combination of low-pass filters with different time constants. The low-pass filter combination, which we refer to as the sensor, uses a low time constant for the first filter and a large time constant for the second filter. The first filter therefore acts as a *rectifier*, and the second filter behaves like an *integrator*. The use of this sensor at the transmitter RF output allows the capture of essential test information through low-speed sampling and is very attractive for area/performance overhead reasons. The sampled response is then fed to the on-board processor for analysis and estimation of key transmitter specifications.

The proposed test technique is conducive to performing concurrent/online testing of wireless transmitters in the field with the available on-board test resources. The sensor can also be used as a *frequency discriminator*, and can be used to perform low-complexity built-in test of frequency sources. The following sections describe the

development of the rectifier-integrator sensor along with the associated test stimulus generation and response capture procedures used to test for phase/frequency modulated transmitters.

3.4.1 Phase/Frequency Modulation Basics

Phase/frequency modulation schemes such as FSK and PSK, respectively, are important in the context of wireless communications due to their simplicity and superior performance in the presence of multi-path effects. In phase modulation, data is transmitted by changing the phase of the carrier depending on baseband data. In frequency modulation, the carrier frequency shifts between discrete values in accordance with the modulating baseband data bit-stream. A phase modulated signal ($y_{PM}(t)$) can be written as

$$y_{PM}(t) = A * \cos[\omega_c t + m * x(t)] \qquad (43)$$

where,

A is the amplitude of the carrier signal, ω_c is the frequency of the carrier, m is the modulation index, and $x(t)$ is the input signal. As observed from Equation (43), the phase of the carrier is modulated by $x(t)$ while the amplitude of the resulting signal remains a constant. A frequency modulated signal can correspondingly be defined as

$$y_{FM}(t) = A * \cos\left[\omega_c t + m * \int_{-\infty}^{t} x(t)dt\right] \qquad (44)$$

Figure 91 shows phase and frequency modulated waveforms along with the digital bit-stream that the modulation represents. As in the case of a phase-modulated signal, the peak-to-peak amplitude of the frequency-modulated signal is constant. The main advantage of using phase/frequency modulation is that it allows the transmitters to be

more power efficient. This is because the envelope of the modulated signal is constant allowing higher quality of transmission in the presence of nonlinearities in the PA.

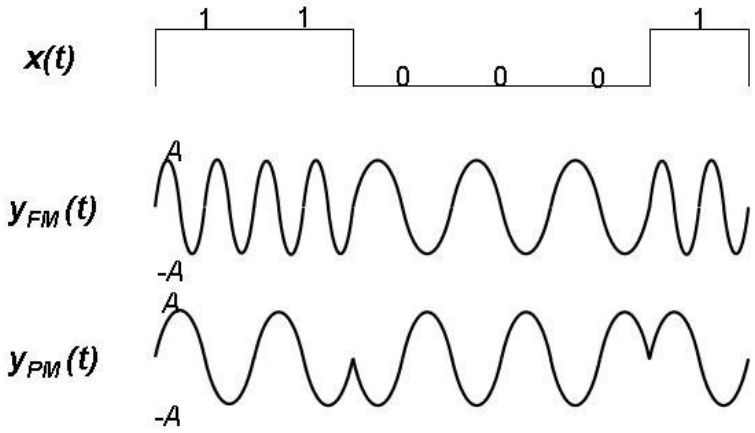


Figure 91 Frequency and phase modulation

Figure 92 shows a typical voltage controlled oscillator (VCO) modulating transmitter architecture, where the carrier RF signal is modulated directly by the VCO. The signal transmitted by the antenna must comply with the emission standards so that it does not interfere with other communication channels. The main cause of the leak of spectral content into adjacent channels is due to the non-linearity in the building blocks of the transmitter.

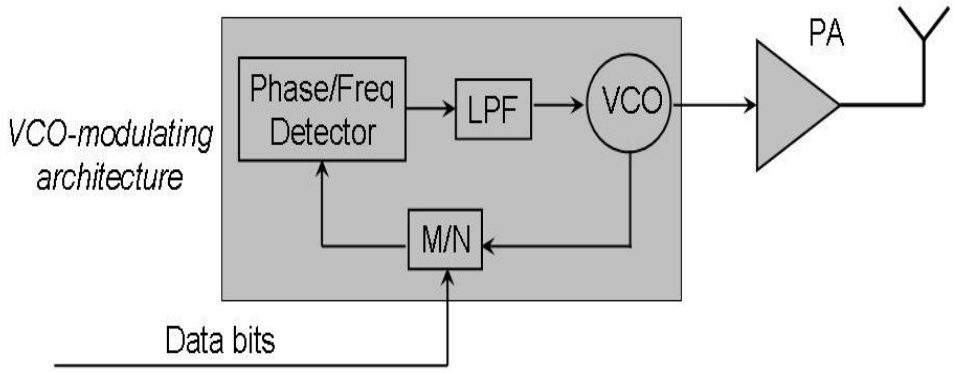


Figure 92 VCO-modulating transmitter architecture

The spectral purity of transmitter is therefore characterized through tests such as ACPR, P1dB, and IIP3. The following section describes a rectifier-integrator sensor and proposes a simple and efficient technique to perform BIT of FSK/PSK devices. The sensor can also be used as frequency discriminator i.e. it can differentiate between different frequencies.

3.4.2 Rectifier-Integrator Sensor

The following section describes the operation of the sensor. The first low-pass filter with a small time constant passes a portion of the positive half of the signal. In other words it behaves like a rectifier. It consists of a transistor (NPN or NMOS) in an emitter (source) follower configuration and an RC combination at the output. During the positive cycle of the input signal, the capacitor is charged and during the second half the capacitor discharges through the output resistor. The resulting rectified waveform is shown in Figure 93. It is to be noted that the input RF signal is not only rectified but is also modified due to the RC charging and discharging at the output. The resulting waveform at the output of the rectifier, when integrated over multiple cycles, produces another waveform that varies depending on the frequency of the input signal. This signal at the output of the integrator (second filter) can then be sampled by a low-speed ADC and analyzed to extract the frequency information of the input signal. Key features of the proposed sensor include its ability to discriminate between different input frequencies as explained above, and also its ability to track and capture information in the input RF waveform, which are the used to estimate transmitter specifications.

This ability of the sensor to track transmitter non-idealities present in a constant-amplitude waveform is discussed later. The theory behind the frequency-discrimination

property of the proposed sensor is described below. If a constant envelope signal such as a sine wave with constant amplitude is fed into an integrator, the output response charges to a value determined by the circuit topology and the voltage of the input signal. Irrespective of the frequency of the input, the output is the same. Therefore, for the sensor to perform frequency discrimination, the signals should be conditioned (modified) such that they contain frequency-dependent characteristics that can in turn be accumulated by the integrator. For this purpose, the input waveforms are passed through the rectifier. As explained earlier, the rectifier passes the first half of the positive cycle of the waveform if the input voltage exceeds the threshold voltage (*Vth*) of the base-emitter junction. During the second half of the positive cycle, the capacitor discharges through the resistor. The output voltage of the rectifier therefore follows an exponential decaying profile during the second half of the positive cycle. The decaying time-constant τ_1 of the output voltage is given by

$$\tau_1 = \frac{1}{R_1 C_1} \qquad (45)$$

It is observed here that the decaying portion of the output waveform is determined by the time constant of the rectifier and the input frequencies. The rectifier output for the two input signals of frequencies *f* and *2f* are shown in Figure 93. It is observed that the area under these output curves is different, and depends on the frequency. It is this frequency-dependent property of the rectifier output that is key to the frequency-discriminating functionality of the sensor.

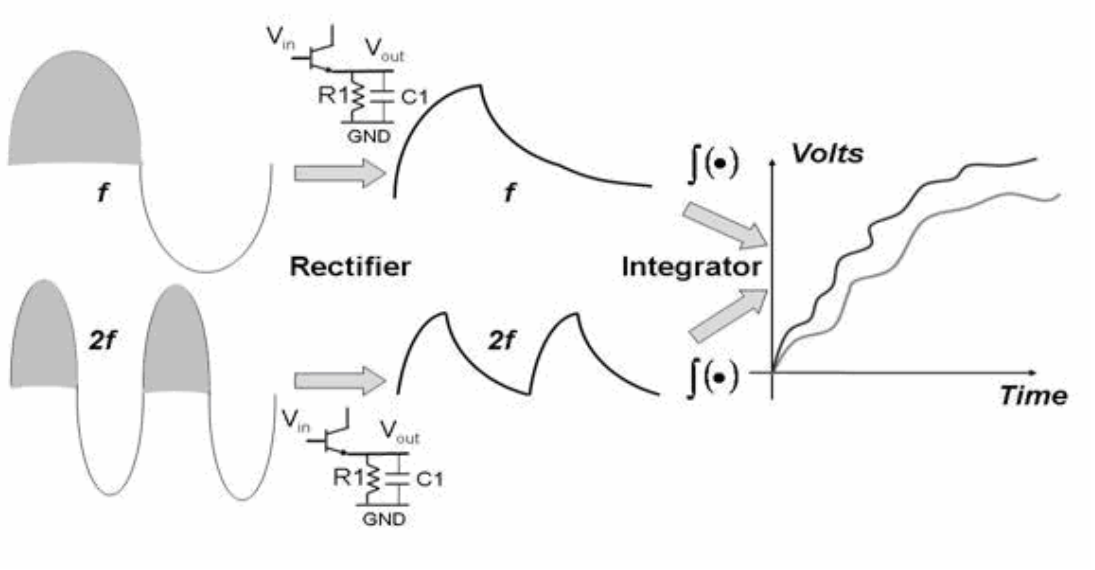


Figure 93 Rectifier-integrator sensor: Frequency discrimination

The topology of the proposed sensor is also shown in the figure. The first stage is the rectifier block. It is an emitter-follower with *R1* and *C1* connected to the emitter. The integrator in the second stage is also an emitter-follower with a different set of elements, *R2* and *C2* at the output. The RC constant of the integrator needs to be much larger than the RC constant of the rectifier. This is because the integrator should accumulate the charge over multiple cycles of the input waveform. The rectifier output, on the other hand should follow the input signal. Hence, the RC constant of the rectifier should be of the order of the input signal time period.

$$(\tau_1 = R_1 C_1) << (\tau_2 = R_2 C_2) \qquad (46)$$

The sensitivity of the sensor (frequency selectivity) depends on other factors including the values of resistors and capacitors, input voltage swing, supply voltage and the transistor widths. It is therefore important to maximize the widths of the rectifier and integrator transistors by adding multiple fingers in parallel. The integrator usually requires more transistors compared to the rectifier due to the relatively larger value of

the capacitance *C2*. Increasing the number of parallel transistors provides a sufficiently large value of the charging current, thereby, increasing the sensitivity of the integrator.

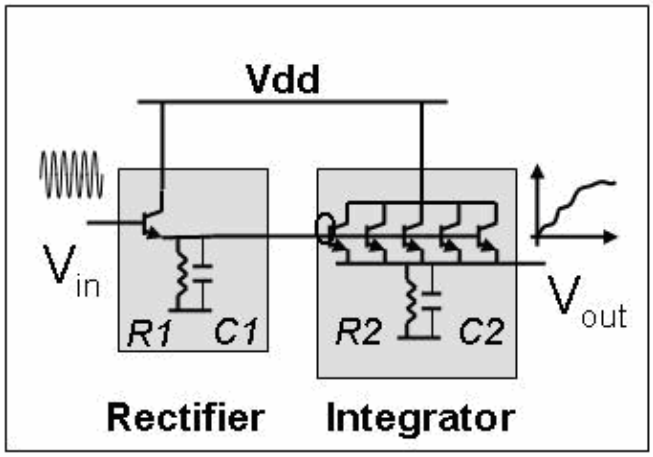


Figure 94 Sensor Schematic

Transient simulations in Agilent ADS are performed on the sensor. Two different input signals of frequencies 1MHz and 2 MHz, respectively, are applied to the sensor (Figure 94). The rectifier and integrator outputs are plotted in Figure 95. As seen from the plot, the rectifier output shows the charging-and discharging pattern. The output signal has smaller swing for the 2 MHz input. Therefore, the average value of the rectifier output is higher for the 2 MHz signal. The corresponding integrator outputs are shown in the plot below. As expected, the integrator output is different for the two frequencies. The difference in integrator output voltages is greater than 50mV after about 10usec. The sensor, therefore, has the ability to discriminate between frequencies of the input signal.

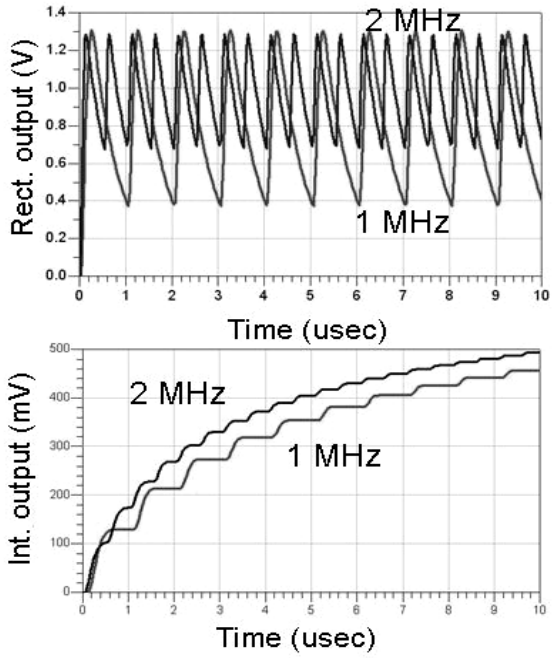
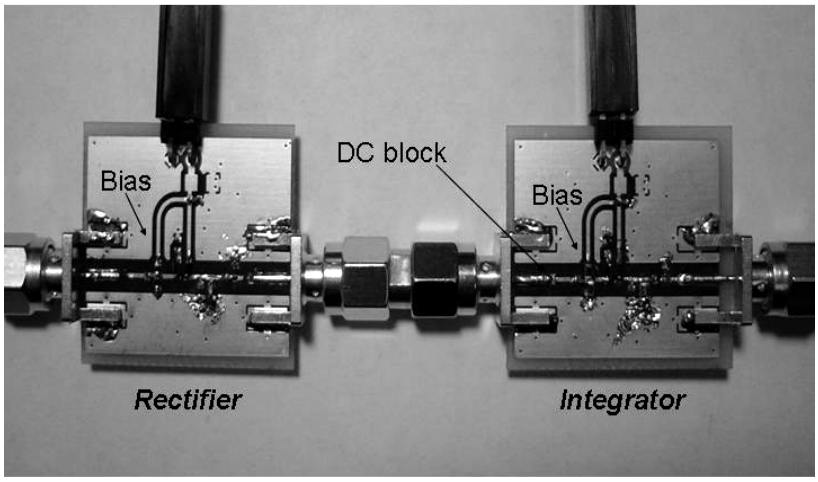


Figure 95 ADS simulations: Rectifier and integrator outputs

Next, hardware measurements are performed to demonstrate the feasibility of using the sensor for frequency discrimination. For this purpose, the rectifier and integrator circuits are fabricated on PCB with FR-4 as the substrate. The photograph of the fabricated sensor is shown in Figure 96. Since the use of multiple parallel transistors for the integrator was not feasible for the board design, it was circumvented with the use a current source at the output of the integrator.



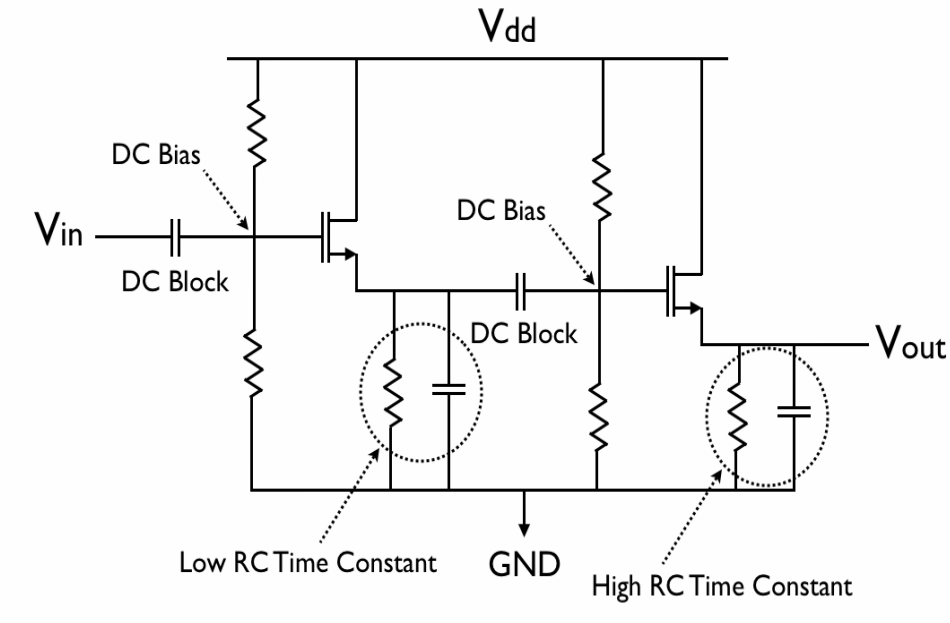


Figure 96 Rectifier-Integrator sensor

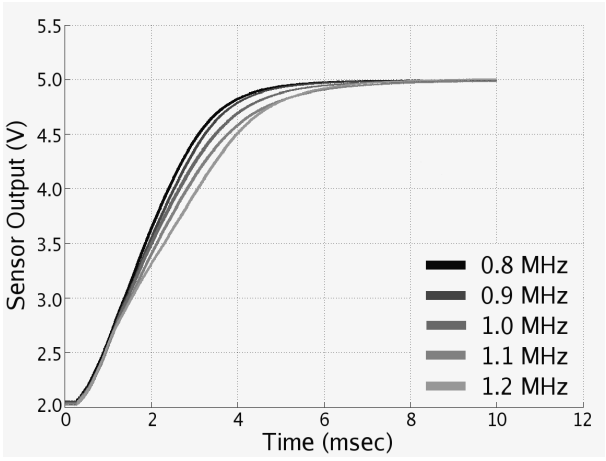


Figure 97 Measurement results: Frequency discrimination

The purpose of using multiple parallel transistors in the integrator is to increase the charging current at the output of the integrator, which in turn increases the sensitivity. The use of a current source at the output achieves the same purpose without the need for using multiple parallel transistors. The DC block at the input of the integrator passes only the transient charging-discharging pattern of the rectifier. Measurement results for the sensor are shown in Figure 97. Five different input frequencies are tested and the resulting output is shown in the plot. As seen from the plot, the sensor discriminates between the frequencies with good resolution as evident from the output charging profile. The sensor output follows different paths for the different frequencies, eventually charging up to the output DC voltage at steady state. The output can be sampled at low frequency using the on-board ADC and analyzed by the baseband processor (in a BIT scheme).

3.4.3 Built-in Test of FSK Transmitters Using Rectifier-Integrator Sensors

In this section, alternate testing of FSK transceivers using the sensor at the output of the transmitter is described. Alternate test is used in this work to test constant amplitude signals (from FSK) transmitters to test specifications such as gain, IIP3, P1dB etc, and also to diagnose and predict its behavioral parameters. The sensor output response captures 'response-features', and this is used to test for the above mentioned specifications using MARS. An FSK modulated signal consisting of two different frequency components are used. Since the generation of a suitable test stimulus is performed in the baseband, the variables include the frequency deviations of the signal, amplitude, and the order of these variations. It was observed that the accuracy of prediction improves if multiple amplitude levels of the test stimulus are used. In our

case, the test stimulus consisted of an FSK modulated signal with two separate amplitude levels as seen in Figure 98. A set of 200 instances of the transmitter are used for generating the MARS function. The 200 instances were generated by perturbing the transmitter behavioral parameters.

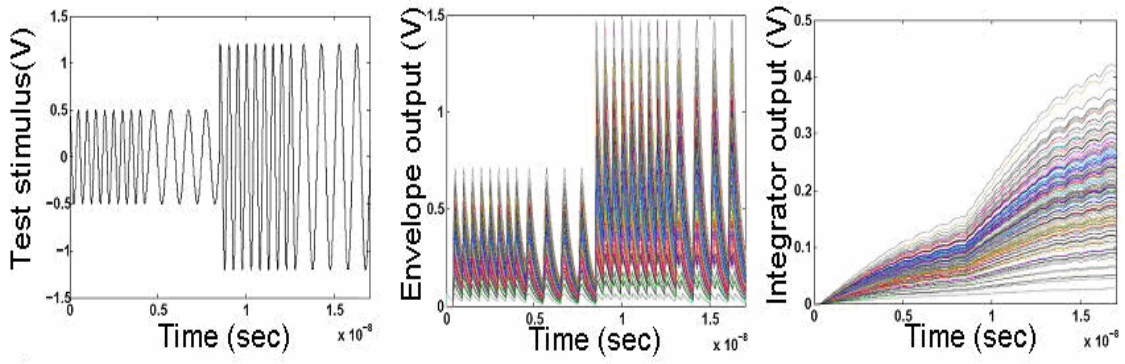


Figure 98 Test stimulus and Test responses

The generated MARS function was then used for evaluating another set of 50 instances of the transmitter in the evaluation phase. Figure 99 shows a plot of the predicted vs. actual values of transmitter specifications – gain, IIP3 and P1dB, for these 50 instances. As observed from these plots, the specifications are predicted with good accuracy (relative error < 4%). Next, the effect of process variations in the sensor on test accuracy is studied. For this purpose, the RC constants and threshold voltages of the rectifier and integrator circuits are randomly perturbed by up to 15%.

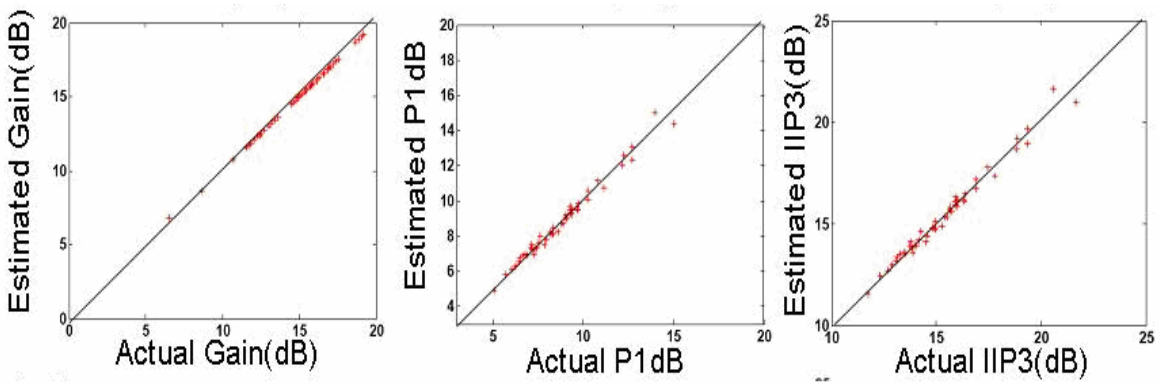


Figure 99 Specification prediction with ideal sensors

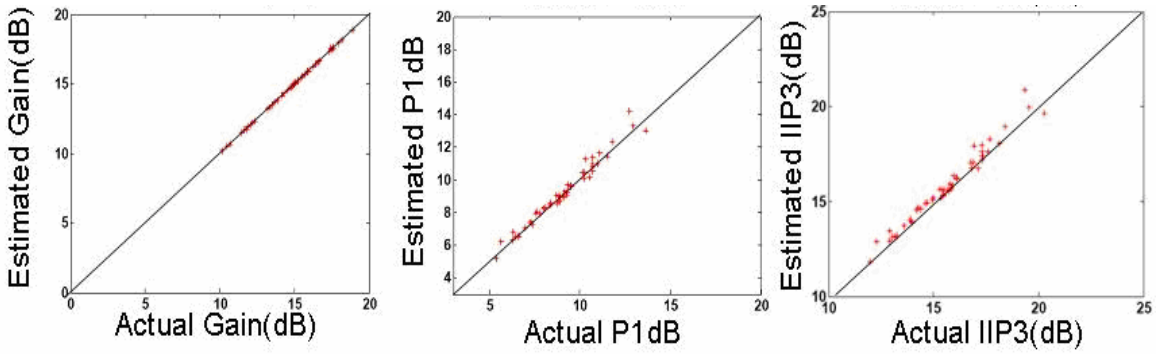


Figure 100 Specification prediction with process-perturbed sensors

The test results for this case are plotted in Figure 100. It is observed from the plots that specification prediction is relatively robust to process variations in the sensor. The relative error was found to be less than 5%. This can be attributed to the frequency-discrimination capability of the sensor and the use of multiple amplitude levels in the test response. Since the sensor response is captured and analyzed by MARS at two different frequencies and amplitude levels, the process variation effects are calibrated out by MARS. Specifically, the use of two frequencies accounts for changes in the RC constants, and the two amplitude levels account for variations in the threshold voltages.

3.4.3.1 Measurement Setup and Results

For hardware validation of the proposed BIT approach, an experimental setup shown in Figure 101 is used. Frequency/phase modulated test stimulus was generated in the PC and fed into the baseband input of the up-conversion mixer through a DAC of a DAQ hardware (National Instruments SCB-68.) The baseband signal of frequency 1MHz is up-converted by the mixer using a carrier signal of 1.0 GHz from a local oscillator (Agilent E4436B) [150]. The proposed sensor is implemented on a separate PCB for the hardware demonstration purpose, and is used to capture the signal at the output of the power amplifier. The sensor output is then sampled at the rate of 1Msps using the ADC of the DAQ hardware and fed back to the PC for analysis and specification prediction. Due to the practical constraint of building 100 different transmitter instances comprising the mixer and PA, the PA power supply variation in the range of 2 to 4 V with 0.02 V increments was used to mimic 100 instances creation. 90 instances from among these were used as a training set for generating a mapping function between the sensor output and the actual transmitter specification using MARS. The validation set consisted of the remaining 10 instances. The sensor data captured from the transmitters in the validation set was then used to estimate their actual specifications. Figure 102 shows plots of the predicted vs. actual specifications (gain and IIP3) of the validation set.

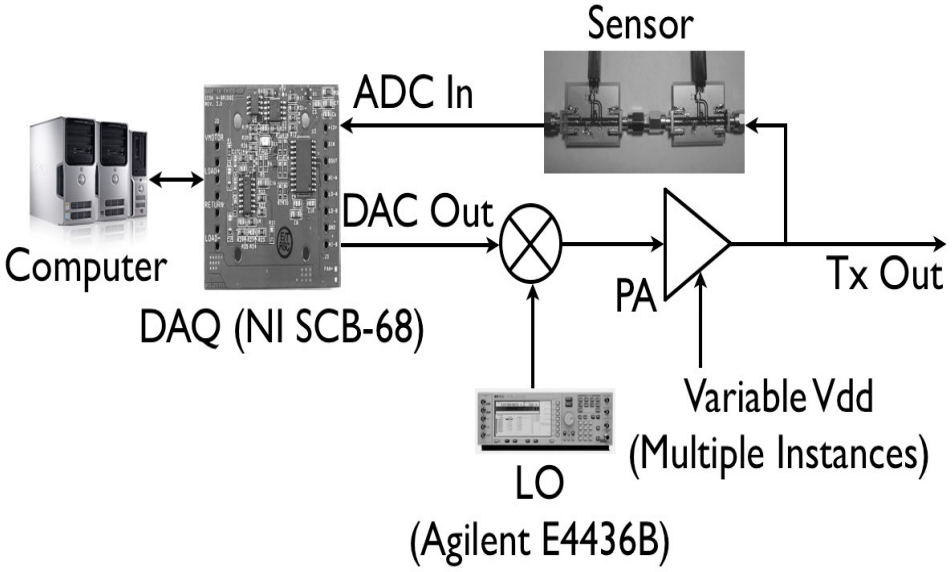


Figure 101 Hardware test setup for transmitter specification prediction

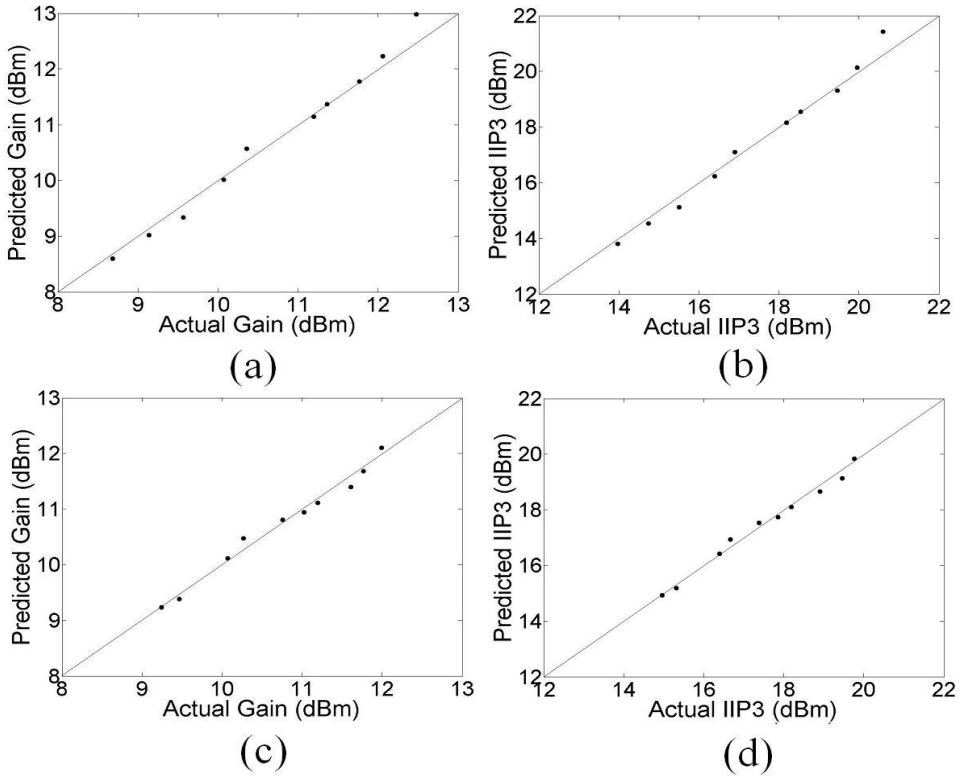


Figure 102 Estimated vs. actual specification of perturbed transmitter instances for FSK modulation: (a), (b), and PSK modulation: (c), (d).

In conclusion, an efficient BIT technique for frequency modulated signals was proposed using a rectifier-integrator circuit as the embedded RF sensor. The output of the sensor is a slow varying integrator charging profile that can be sampled using the on-board ADC. The proposed sensor has the ability to discriminate between different frequencies, and therefore, can be used as a low-cost option to test devices such as VCOs, PLL etc. The rectifier-integrator sensor can also be used to perform specification testing of the frequency modulated transmitters. Good test accuracy was observed, thereby, demonstrating the feasibility of the proposed approach to perform efficient specification testing of frequency modulated transmitters.

Chapter 4

LOW POWER OPERATION OF WIRELESS TRANSCEIVERS

Modern wireless transceiver systems are often over-designed to meet the requirements of low bit error rate values at high data rates under worst-case channel operating conditions (interference, noise, multi-path effects). This results in circuits being designed with "sufficient" margins leading to lower efficiency and high power consumption. In this Chapter, an adaptive power management strategy for RF systems that optimally trades-off power vs. performance for the RF front-end to maintain operation at or below a specified maximum BER across temporally changing operating conditions is presented. In this scheme, more power is consumed by the RF front end when the communication channel degrades, and vice versa. Since the maximum bit-error rate specification is not violated, minimum voice or video quality through the wireless channel is always guaranteed.

The key idea of the work presented in this chapter is to exploit built-in design margins in wireless systems across temporally changing channel conditions to save power. For this purpose, a suitable adaptation metric that quantifies the cumulative sum of the quality of transmission (this is well controlled at the radio base station), the channel quality degradation and the quality of signal reception, is chosen. The *adaptation metric* is computed by the baseband signal processor in real-time (online). When this adaptation metric has a "high" value (high fidelity of the received signal) the quality of signal processing in the RF front end (i.e. its performance) can be degraded

intentionally by reducing its supply and bias voltages dynamically to save power while maintaining a specified maximum BER. In this case, EVM is chosen as the adaptation metric as explained later.

In the proposed approach, the wireless front-end always strives to operate at the lowest power consumption levels (lower performance) for any specified modulation. The use of such a feedback control technique to adapt to dynamically changing air channel conditions saves significant amount of power whenever the channel quality is not worst-case (while satisfying the BER condition). A corollary of this approach is that as channel degrades, with the use of appropriate feedback control techniques for controlling the supply and bias voltages, the same receiver will automatically consume more power in an effort to make up for decreased channel quality. The above mentioned concepts are demonstrated using an OFDM receiver front end as the test vehicle.

4.1 WIRELESS RECEIVER DEVELOPMENT

Circuit-level implementations of the LNA and mixer are realized and ADS simulations are performed for various supply and bias settings to characterize their performance. The data from these simulations is then used to develop behavioral models, which are used for system-level study of the proposed approach. The behavioral modeling of key components in the OFDM receiver module and channel is presented.

4.1.1 LNA and Mixer Circuit-level Implementations

A wideband LNA is designed in CMOS 0.18u technology. A common gate input stage provides good input matching over a wide range, the common source intermediate stage provides the required gain, and the class A output stage provides good signal

swing. The operating range of the designed LNA is from 2-7 GHz, and the gain is observed to be 16 dB at 2.4GHz for a nominal supply voltage of 1.8V and bias of 0.8V. The LNA has NF of about 3dB, and the total DC power consumption of the LNA is about 25.6mW. For the mixer, a double-balanced Gilbert cell architecture was chosen. A balun is used for single-to-double ended conversion. The mixer provides a gain of 11.8 dB, NF of 8 dB. The operating range of the mixer is from 2-7GHz, and the power consumption of 6.6mW at a nominal supply voltage of 1.8V and bias of 0.8V. The schematics and the power vs. supply/bias contours for the LNA and mixer are plotted in Figure 103.

The power consumption of the LNA and mixer decreases with the lowering of supply and bias voltages, but trades-offs with gain, non-linearity, and NF specifications. This, in turn affects the system-level performance. For this work, the set of supply (V_{ddL}, V_{ddM}) voltages used for adaptation .is given by the set [1.8 1.6 1.4 1.2 1.0]**.** The corresponding set for bias voltages (V_{bL}, V_{bM}) is given by [0.8 0.7 0.6 0.5]. The modeling of the LNA and mixer non-idealities is realized through a non-linear transfer function as explained in Chapter 3. For the mixer, in addition to the non-linear transfer function implementation, the frequency mixing operation is realized by a simple multiplication operation. Transistor-level simulation data for the LNA and mixer obtained from the Agilent ADS tool is used to extract the coefficients of the LNA and mixer transfer functions. The transfer functions are generated for all the possible combinations of supply and bias voltages.

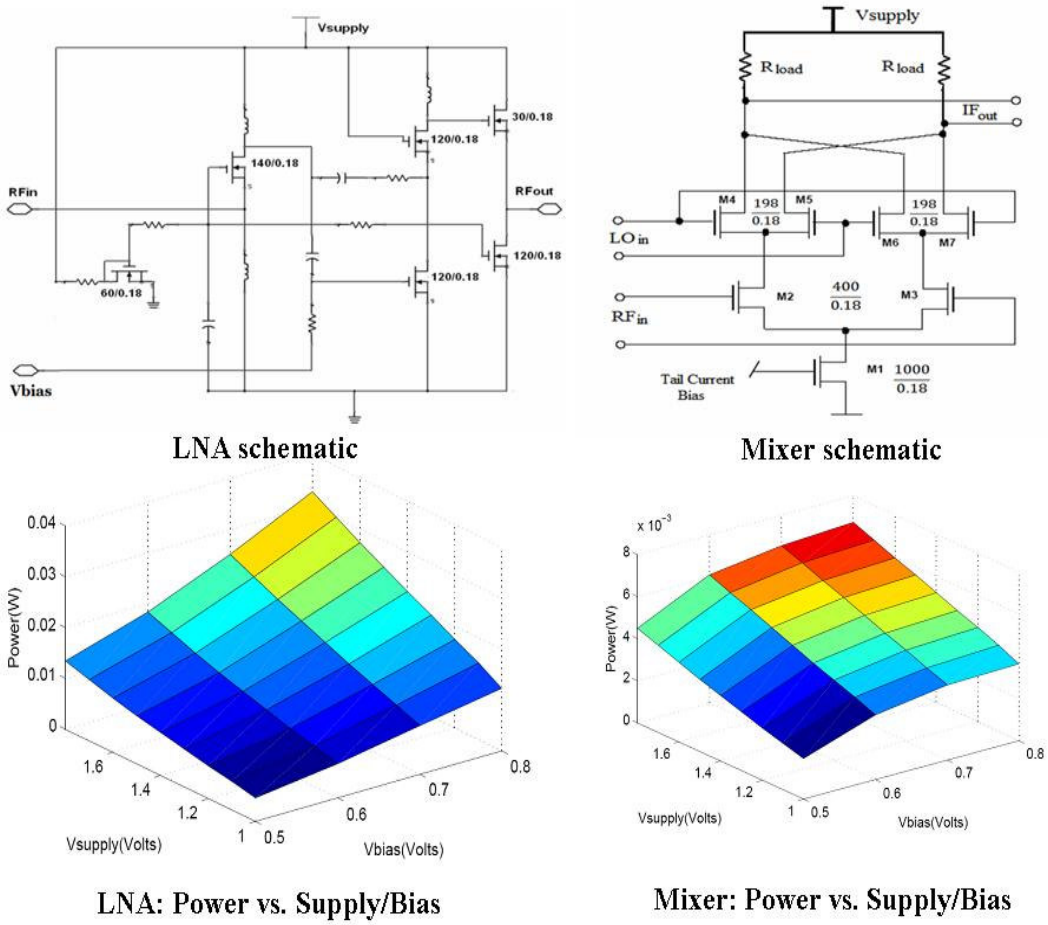


Figure 103 LNA and Mixer circuit schematics and power consumption profiles

The choice of supply and bias voltages of the LNA and mixer constitute a total of 400 different settings. Behavioral parameters of the RF front-end are extracted for each of these 400 configurations for use in the simulation study. It should be noted here that many of these 400 configurations are not optimal from a power consumption standpoint. Therefore, the set of configurations are pruned down to a limited set of optimal values using a multi-dimensional optimization approach in the design phase (as explained later). The reduced set of supply and bias voltages are used to dynamically configure the RF front-end during run time for minimizing power across changing environmental conditions using an optimal control law.

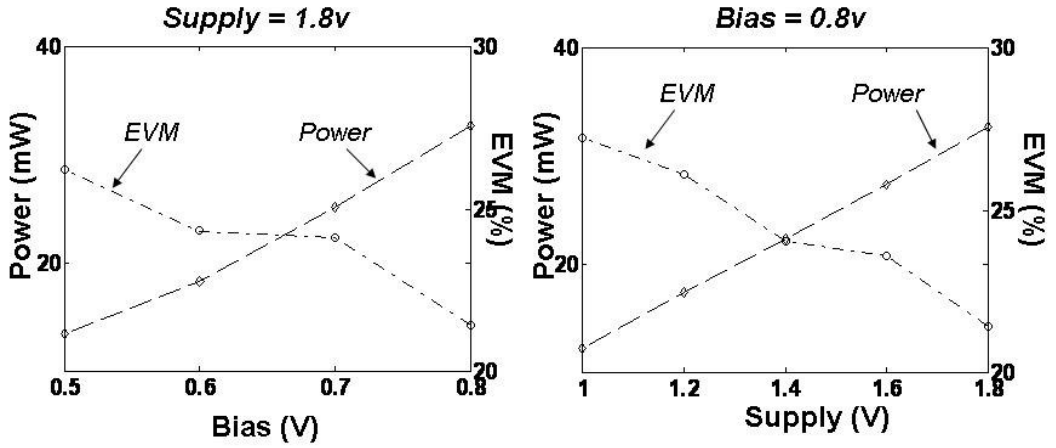


Figure 104 Variation of LNA power consumption and system performance for varying supply and bias voltages

To justify the use of supply and bias as control knobs in the RF front-end, the effect of varying supply and bias on EVM, which quantifies the system, is studied. Figure 104 plots the variation of LNA DC power consumption and EVM specification for varying supply and bias voltages. It is seen that the power consumption decreases monotonically as the supply and bias voltages are reduced. Though the EVM specification increases in general with reducing supply and bias voltages, the trend may not be monotonic.

4.1.2 Baseband Functionality

The baseband functionality was implemented in MATLAB as explained in the previous chapter. At the transmit end of the OFDM baseband, input serial data stream is formatted into the word size required for transmission, e.g. 2 bits/word for QPSK, 4 bits/word for 16-QAM, and 6 bits/word for 64-QAM. The data is converted to parallel format and sent to an IFFT block. The IFFT block converts the parallel modulated data to the corresponding time waveform (symbol) that is transmitted. The receiver portion

performs a reverse operation on the received signal - serial-to-parallel conversion followed by FFT to obtain data bits.

4.1.3 Channel Modeling

The effect of the channel includes the sum contribution of the air-antenna interface effect at the transmitter and receiver, respectively, and the effect of the physical medium (air) between the transmit and receive antennas.

- Propagation loss and noise addition are modeled as a simple attenuation of the received signal followed by addition of white noise to the received signal.
- The multipath and fading effect are modeled using an FIR filter. The length of the FIR filter determines the maximum delay spread in the channel.
- Interference is modeled as a combination of adjacent channel interference and microwave interference. Adjacent channel interferer is modeled as an OFDM signal in a neighboring band. Emissions from this band affect the signal in the band of interest (2.4GHz). The adjacent channel interferer is given by

$$i\_adj(t) = f(A(t), f_c(t))_{OFDM} \qquad (47)$$

where A(t) is the time varying amplitude and fc(t) is the time varying frequency. The microwave interferer is modeled as an AM-FM source that allows the characterization of frequency wander based on the work presented in [151]. AM-FM modulation is employed on a time-varying sinusoidal signal to generate the microwave interferer. The frequency of the microwave interferer is given by

$$f_d(t) = f_0 + f_w \sin\left(\frac{2\pi t}{T_w}\right) \qquad (48)$$

where f_o and f_w are initial interferer frequency and the maximum frequency wander, respectively, and T_w is frequency wander period. For this work, fo is 2.412GHz, f_w is 20MHz, and T_w is chosen as 20ms.

4.2 CHOICE OF ADAPTATION METRIC

The choice of the adaptation metric is driven by the requirement that it should encompass the sum effect of non-idealities in RF front-end/analog blocks, channel effects and noise etc. In other words, the adaptation metric must provide the best indication of the system performance under all possible environmental conditions. The performance of a communication system is usually quantified in terms of the BER of the system. BER gives the rate at which errors occur during communication. Typical values for wireless systems are in the order of 10^{-3}-10^{-4}. Measuring the BER of a system typically incurs a long time as several thousand bits are transmitted and received.

A metric (system specification) that can easily measured in DSP using less time, and which strongly correlates to the system BER specification is highly desirable. The choice of EVM as an adaptation metric in a tunable word length OFDM receiver was explored in [152]. EVM, like BER is an at-speed specification of a wireless system i.e. it is measured during the actual operation of the device. EVM can be easily calculated for each data frame of the received signal. System-level simulations were performed to ascertain and establish a relationship between the EVM and BER specifications. Figure 105 plots the EVM and BER for a wireless system under different channel conditions and system non-idealities. Three different modulation schemes used in practice – QPSK, 16-QAM, and 64-QAM were employed for evaluation purposes and about 10^5 bits were transmitted and received.

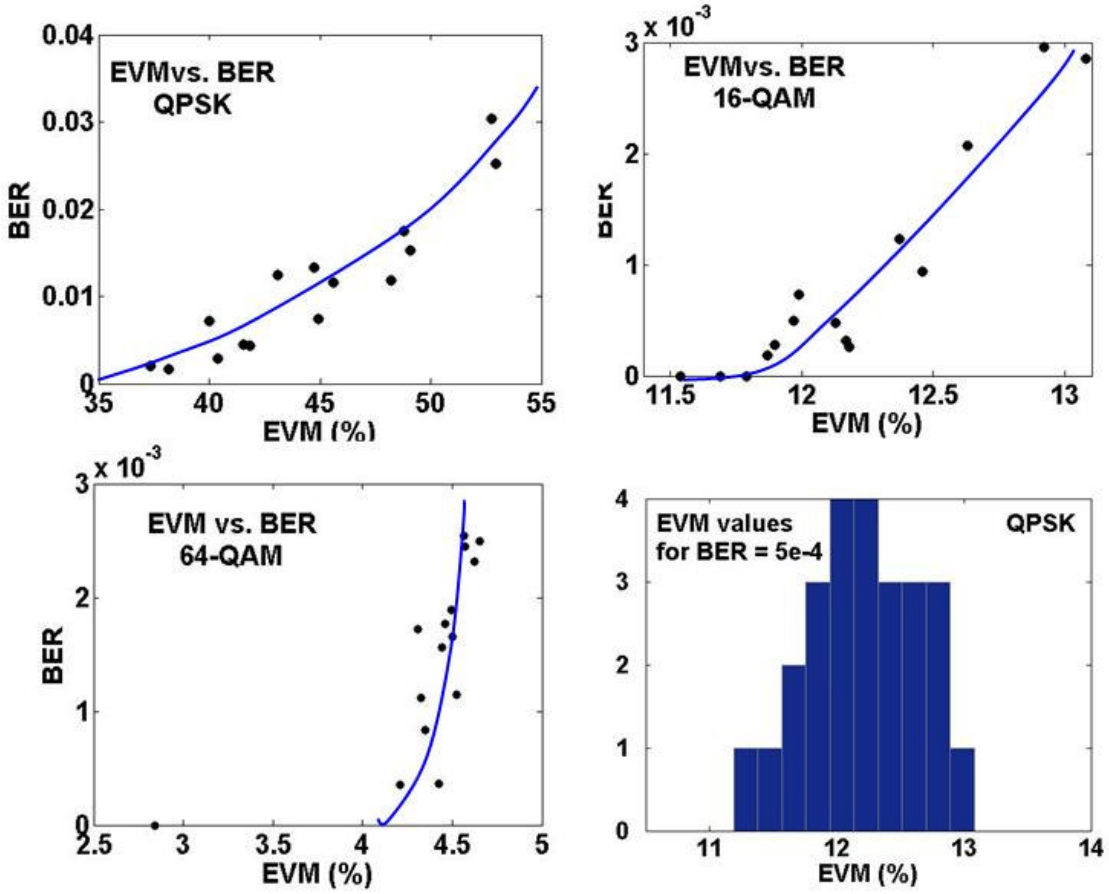


Figure 105 EVM vs. BER relation: System-level simulations

The different values of EVM and BER are obtained by perturbing channel conditions and the RF front-end non-linearities. From the plots it is observed that in general an increase in EVM is associated with an increase in BER, and vice versa. A relationship between the two specifications can therefore be established. An upper bound on the BER specification can then be translated into an upper bound on the EVM. For example, if BER bound is set at 5e-4, the corresponding mean EVM bound for the QPSK, 16-QAM, and 64-QAM cases can be approximated to about 35%, 12%, and 5% respectively. Moreover, it should be noted that the EVM specification is determined by random processes in the channel and the device among other factors. A simulation was therefore performed to analyze the repeatability. Figure 105 also plots the histogram of

the obtained values for QPSK modulation at a fixed BER of 5e-4. The experiments were repeated 25 times. The 3σ variation of the EVM value is accounted for in setting the *threshold value* and a *guard band* around it for any desired BER value.

Figure 106 shows the constellation diagram for QPSK encoded symbols. As the channel conditions and receiver performance degrade, the constellation points for each symbol lie inside circles of increasing size, corresponding to increasing EVM. When the circles cross the horizontal and vertical constellation boundaries, the received symbols are decoded incorrectly and bit errors occur. Theoretically, one could leave a safety margin and operate within the largest circle determined by the safety margin without causing bit errors. However, even for conservative designs, periodic bit errors do occur in practice. Hence, the safety margin is determined by the maximum specified bit error rate (BER). Under feedback control, the receiver will operate within the boundary of the largest circle not crossing the specified safety margin for the constellation diagram.

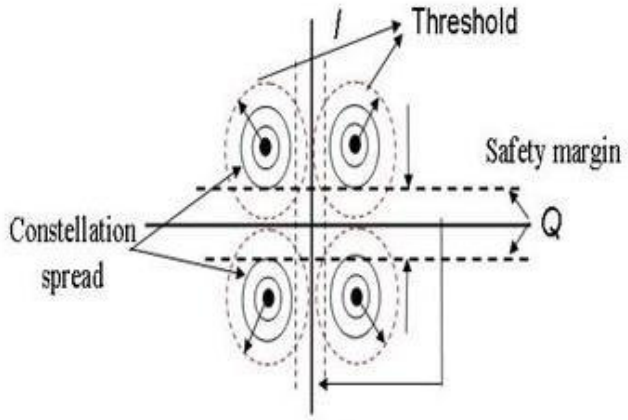


Figure 106 QPSK guard and threshold estimation

4.3 PROPOSED APPROACH FOR MINIMUM POWER OPERATION OF THE RECEIVER

In this section, the proposed approach for minimum power operation is described from a system-level perspective. The system under consideration consists of the receiver RF front-end and the baseband processing module that dynamically evaluates the performance metric for received OFDM symbols, and operates the RF front-end close to the error threshold through feedback control. Figure 107 shows the flow chart of required iterations during the design and characterization phase as well as the control scheme during the run time operation of the device. During the design and characterization phase, first a set of tunable control 'knobs' are identified that trade-off the device performance with power consumption. For our purpose, the supply and bias voltages of the LNA (V_{ddL}, V_{bL}) and the mixer (V_{ddM}, V_{bM}) are used as the control parameters. A finite set of channel conditions that adequately span the range 'good' to 'bad' are modeled. The different channels are obtained by perturbing the different channel parameters (noise, multipath components, and interference sources). For each of these channel conditions, the optimal set of tuning parameters are computed through co-optimization for the power and EVM metrics as described below. The computed optimal set for different channel conditions define an optimal locus of tuning parameter values corresponding to the lowest power consumption for maximum allowed EVM. During run time operation, the control law running in the DSP operates the system along this optimal locus for varying channel conditions.

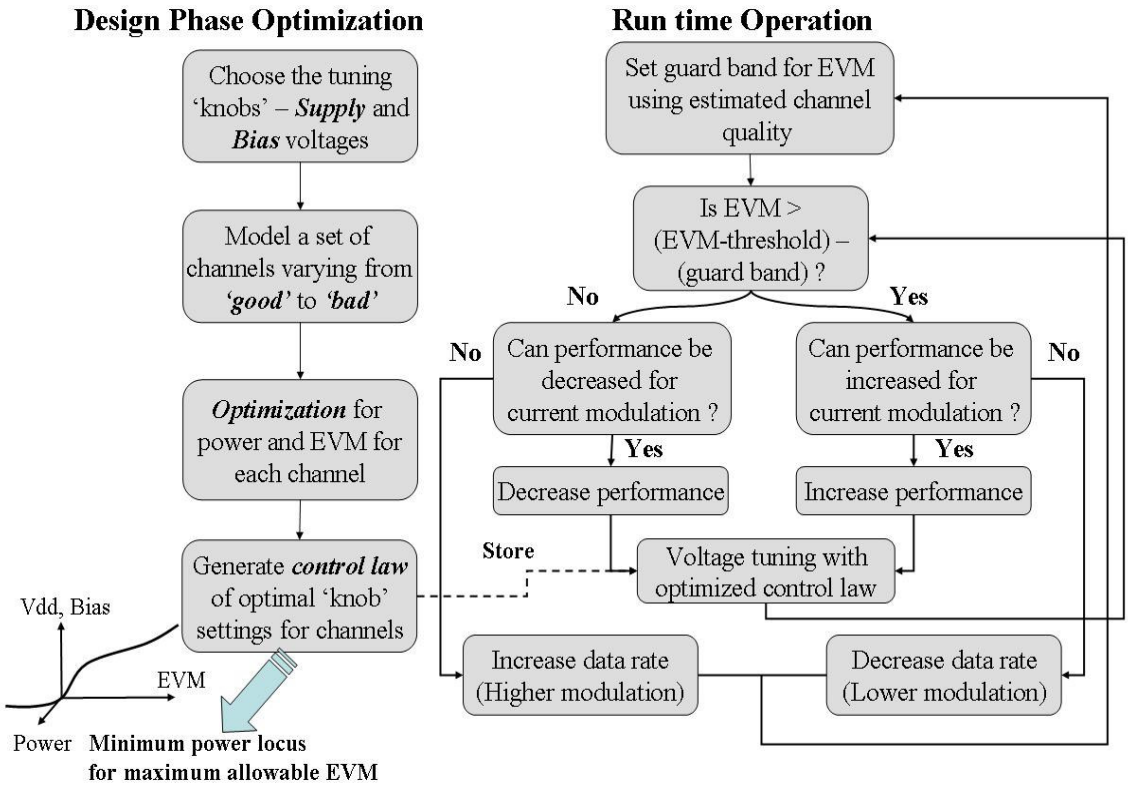


Figure 107 Proposed feedback-driven approach for low-power operation

4.3.1 Power and EVM Optimization

The development of the optimal power control law is summarized below

Input: Maximum allowed EVM for each signal modulation (QPSK, QAM-16,-64).

Goal: For each signal modulation, find V_{dd}, V_{Bias}, tuning = ***f****(channel quality)* such that *power is minimized* and *EVM = EVM threshold-EVM guard band*

The steps are outlined below.

(1) For a given channel, starting from the nominal set of values for the supply and bias voltages (V_{ddL}= 1.8V, V_{bL}= 0.8V, V_{ddM}= 1.8V, V_{bM}= 0.8V), the following adaptation matrix (*M*) is calculated

$$M = \begin{bmatrix} \frac{\partial p}{\partial V_{ddL}} & \frac{\partial p}{\partial V_{bL}} & \frac{\partial p}{\partial V_{ddM}} & \frac{\partial p}{\partial V_{bM}} \\ \frac{\partial EVM}{\partial V_{ddL}} & \frac{\partial EVM}{\partial V_{bL}} & \frac{\partial EVM}{\partial V_{ddM}} & \frac{\partial EVM}{\partial V_{bM}} \\ \frac{\partial p}{\partial EVM_{ddL}} & \frac{\partial p}{\partial EVM_{bL}} & \frac{\partial p}{\partial EVM_{ddM}} & \frac{\partial p}{\partial EVM_{bM}} \end{bmatrix}$$

For example, $\frac{\partial p}{\partial V_{ddL}}$ and $\frac{\partial EVM}{\partial V_{ddL}}$ denotes the change in power consumption and EVM metric for a unit change in supply voltage of the LNA (V_{ddL}), and likewise for other entries in matrix *M*. The third row of the matrix is obtained through a simple ratio of these two quantities. It is to be noted then that each entity in the third row of matrix *M* provides an estimate of the change in power consumption of the circuit for a unit change in the EVM metric.

(2) The tuning parameter for each iteration is then chosen by selecting the maximum of the four entities in the third row. This allows the tuning of the voltage parameter that produces *the maximum reduction in power consumption for the least increase in EVM*.

(3) Once a particular voltage parameter is selected, it is scaled down to generate a new set and matrix *M* is recomputed, and the procedure is repeated.

(4) The iteration steps continue until the EVM threshold condition is violated or all possibilities are exhausted. Thus, an optimal voltage set (V_{ddL}, V_{bL}, V_{ddM}, and V_{bM}) is obtained for each channel condition.

(5) These values are then stored in a LUT in the DSP for adaptation during the online operation of the wireless device.

4.3.2 Run-time Operation of the Device

During run operation, the voltages are continuously scaled down to reduce power consumption of the device for every data rate (modulation). With the scaling down of the voltages, the system-level performance metric (EVM) degrades. This is allowed to continue until the EVM is within certain pre-defined threshold value. Guard band for the EVM threshold is set based on the channel quality. For example, a poor channel would have a larger guard band and vice versa. After this, the performance (supply and bias voltages) of the RF front-end is increased or decreased for the current data rate depending on the computed EVM. The voltages are scaled up or down based on the optimized control law stored in the lookup table. The device power consumption, thus hovers around the lowest possible value for which received signal quality meets the required specification. This scheme achieves significant power savings by operating the system at the lowest possible power for all channel conditions using closed loop feedback control.

4.4 SIMULATION RESULTS AND INFERENCES

Simulations were performed on the receiver system to obtain the optimal voltage set for different channels. The system was first simulated for QPSK modulation, and then for 16-QAM modulation. A set of 12 different channels *(Channel 1(best) – Channel 12 (worst))* was modeled for study purposes. The optimal voltages obtained from the simulations for various channels are plotted in Figure 108. The received QPSK and 16-QAM constellations for nominal voltage operation, and at optimal voltage values (EVM metric close to the threshold) are shown in Figure 109.

As observed from Figure 108, the computed optimal voltage set varies between

the nominal (0.8V, 1.8V, 0.8V, 1.8V) to the lowest possible values (0.5V, 1.0V, 0.5V, 1.0V) over the different channel conditions. It is seen that for a majority of the channel conditions, the receiver operates at the lower than nominal voltage values allowing for significant savings in device power consumption. It is also observed that the optimal voltage values and the associated power consumption is lower for QPSK-modulated signals compared to 16-QAM. This is due to the tighter requirements on the signal quality and SNR for a 16-QAM signal (higher data rates).

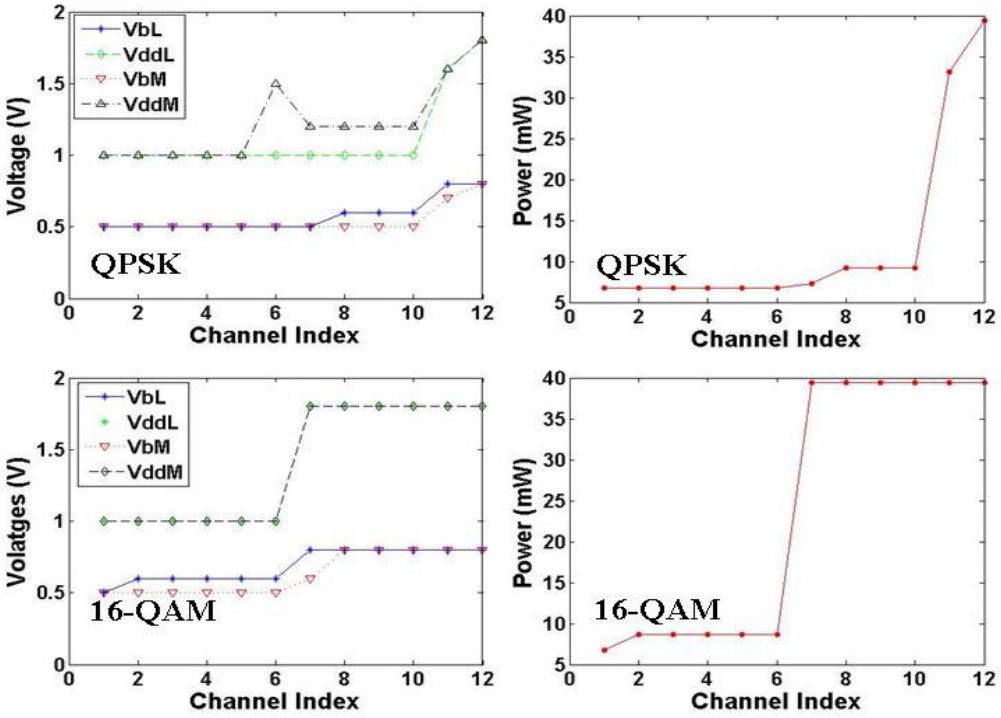


Figure 108 Optimal supply and bias voltages and power consumption for different channel conditions

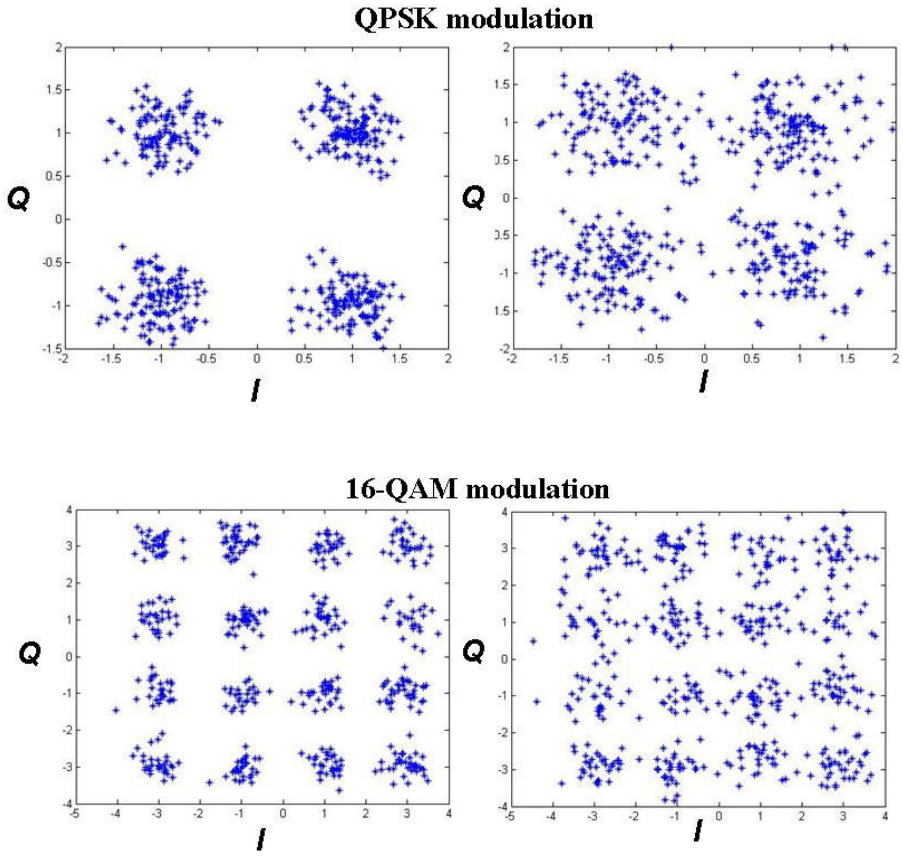


Figure 109 Constellation degradation with voltage scaling

The plots shown in Figure 109 highlight the key advantage of the proposed approach – exploitation of the design margins to operate the device at the threshold. In the absence of feed-back driven adaptation, the receiver system always operates at nominal voltage levels (power = 40mW), whereas in the proposed approach the power consumption tends towards 40mW only for certain channels (only *Channel 12* for QPSK modulation). For good channels, QPSK modulation requirements are met at RF front-end power levels of just 6.6mW (16.5% of the nominal power).

In present-day wireless systems, the data rate (modulation) is dynamically changed by the higher-level protocol depending on channel conditions. For example, the modulation is changed from QPSK to 16-QAM (higher data rates) if the channel

conditions are good. Due to the shift in modulation, the power savings that can be obtained is reduced (due to tighter requirements of 16-QAM) in favor of higher transmission rates. However, the feedback-driven control then ensures that the device operation is optimal for 16-QAM modulation. Thus, the proposed approach enables the receiver operation at lowest *(virtually zero margin)* power consumption levels for all modulations under temporally varying environmental conditions.

4.4.1 Effect of Process Variations

Process variability causes the performance metrics of manufactured devices to vary from the nominal values. The effect of process variability on the power consumption in the proposed adaptation scheme is shown in Figure 110. A set of 50 perturbed instances of the LNA and mixer were simulated in ADS and the corresponding behavioral parameters were extracted for simulations in MATLAB. The adaptive run time feedback control was then implemented for the set of 50 devices, for 4 different channel conditions. Figure 110 plots the variation in the optimal power consumption metric among the 50 perturbed instances for different channels.

The feedback control scheme operates the perturbed devices along the optimal locus for each channel based on the control law. Though the optimal control law (supply and bias control) stored in the LUT is obtained for a nominal device during characterization phase, it is still effective in operating different process-skewed devices at reduced power consumption levels. This is feasible due to the feedback-driven control mechanism that is employed to tune the tuning knobs of the device. Thus for all the 50 perturbed devices, the voltages are regulated such that the operation is close to the error

boundary. The amount of power savings for each device depends on its process spread and its correlation to the optimal locus obtained for a nominal device.

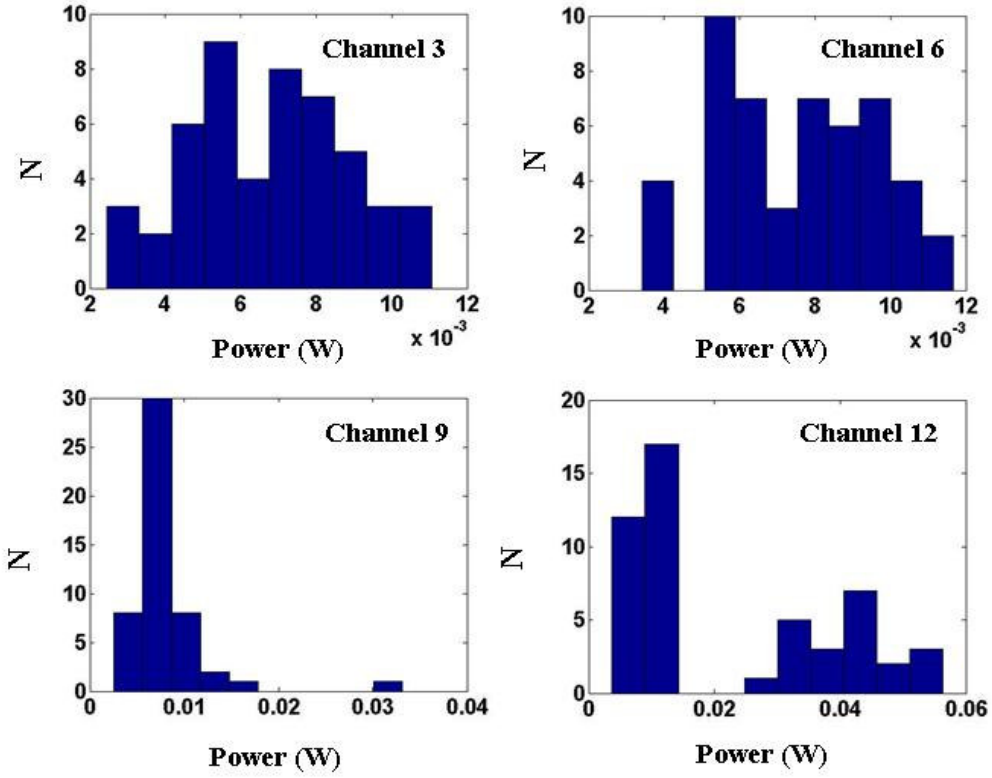


Figure 110 Effect of process variations on the receiver power consumption for different channel conditions

4.5 EXTENSION OF THE APPROACH TO INCLUDE MULTIPLE TUNING PARAMETERS

A preliminary investigation on the feasibility of EVM-driven adaptation for RF circuits (LNA and mixer) was discussed earlier. In this section, a comprehensive system-level framework is presented that dynamically adapts the device to save power in the RF as well as digital blocks. For this purpose, a *multi-dimensional control law* is developed for adaptation of system control 'knobs'. The control law operates the control knobs of

the device such that *minimum power is consumed* across all operating conditions without compromising the bit-error rate (BER) specification. Further, the effect of performing baseband processing (compensation) on the received signal on power consumption of the device is studied. The DSP control also intelligently adapts these control parameters whenever possible by monitoring channel conditions (feedback from adaptation metric).

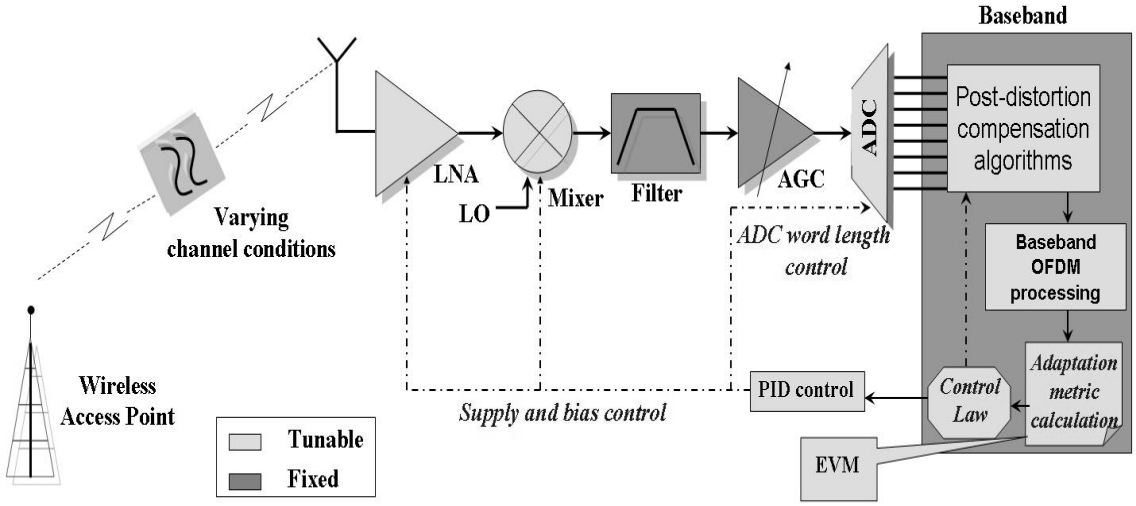


Figure 111 Multi-dimensional power management for wireless receivers

An illustration of the proposed approach for minimum power operation of the receiver is shown in Figure 111. In addition to the tunable supply/bias voltages for LNA and mixer, ADC word length and digital compensation serve as control 'knobs' for system. Theoretically, many more knobs could be included to achieve tunablity. Tradeoffs between the complexity and the amount of power savings obtained should be considered though. The receiver can be operated in several different configurations based on the settings of these control knobs. During the run time operation of the receiver, the performance is periodically evaluated through the computation of a suitable adaptation metric. To do this, the received data at the baseband is first compensated to calibrate-out the effects induced by the RF front-end in its configuration. The control

block then uses this information to set the new configuration of the front-end and ADC word size for optimal power consumption while ensuring that the system-level performance metrics are not violated. This circuit-level energy flexibility comes at limited increase in the area cost and complexity. The optimization procedure described in Section 4.2.1 is extended to include ADC word size as an additional parameter. The optimization is then run to obtain an optimal set of these control 'knob' values for different data rates and channel conditions.

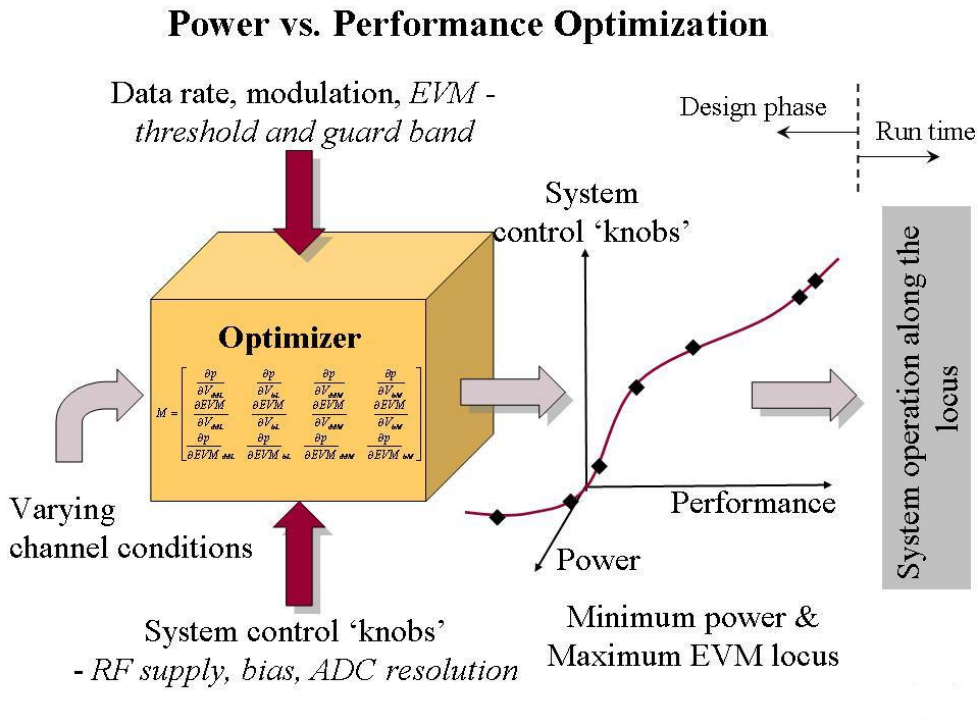


Figure 112 Multidimensional optimization

4.5.1 Digital Compensation for RF Front-end Effects

The performance of the LNA and mixer (gain, non-linearity and distortion parameters) trade-off with power consumption as the supply and bias voltages are scaled. If the relation between RF front-end non-linearity and tuning knob values is characterized prior hand, this information can be used to perform online compensation of

the received data in the baseband using post-distortion algorithms. In this work, inverse transfer function characteristics for LNA and mixer are extracted from ADS circuit simulations for the optimized (pruned) set of supply and bias voltages. They are stored in the look-up table in the DSP for digital compensation during run time operation. The procedure is illustrated below in Figure 113

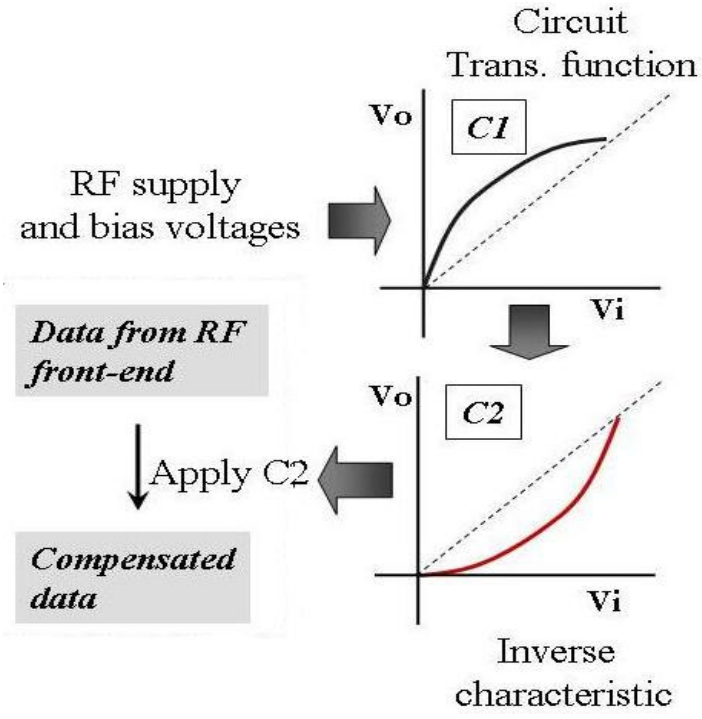


Figure 113 Digital compensation for RF front-end effects

4.5.2 System Simulations

The power-EVM optimizer was simulated to obtain a set of optimal control 'knobs' under a set of channels. The optimizer was run for three different modulations commonly used in practice – QPSK, 16-QAM and 64-QAM. It is observed in Figure 114, for a majority of the channel conditions, the optimal RF power and ADC word size was lower than nominal values – *48mW RF power and 8 bit ADC word size*. It is also observed that the optimal control knob settings and the associated power consumption is

lowest for QPSK modulation. This is due to the tighter requirements on the SNR for 16-QAM and 64-QAM (higher data rates). Simulations also indicate that sufficient margin exists for ADC word size (maximum of 8 bits) pruning under favorable channel conditions. Up to 2 bits of resolution can be sacrificed for QPSK modulation under majority of the channel conditions (Figure 114 (b)). Though the margin is lower in the case of 16-QAM and 64-QAM modulation, the system budget allows for a bit drop under good channel conditions.

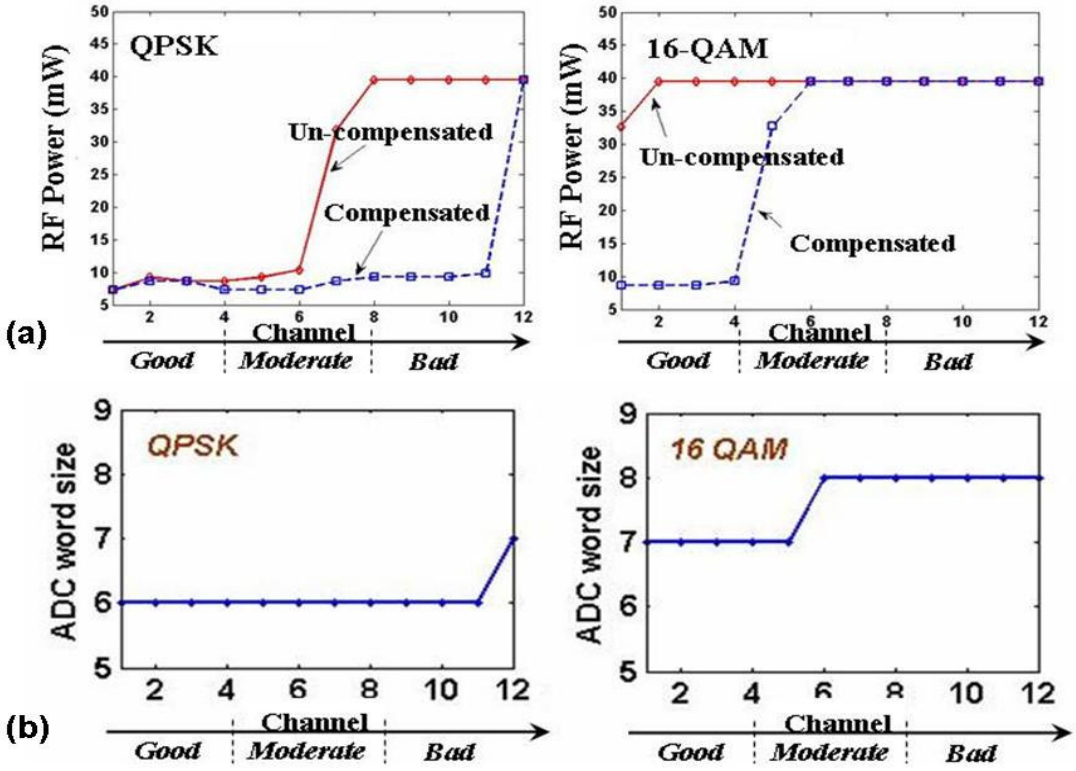


Figure 114 (a) QPSK and 16-QAM RF power consumption for different channel conditions (compensated and uncompensated) (b) QPSK and 16-QAM optimum ADC word size for different channels

Next, run time operation (QPSK and 16-QAM) is simulated by running the optimal control law, first without digital compensation, and then with digital

compensation. It is observed that when digital compensation is performed, more power is saved under moderate and bad channel conditions compared to the uncompensated case. In wireless standards such as WLAN, the higher-level radio link control (RLC) protocol dynamically changes the data rate (modulation and coding) based on the channel conditions. The control law operates within the framework of RLC protocol by operating the device near the threshold for each data rate. From simulations, the computed upper and lower bounds of EVM specification for QPSK modulation are 35% and 12%, respectively, for a BER compliance of 5e-4. Within the QPSK modulation, there exits an EVM margin of 23%-Δ_1- Δ_2, taking. into account the guard band limits. This existing margin is exploited to save power in our approach. From our simulations, it was observed that up to 20mW (25%) of power could be saved by exploiting this margin under QPSK for a guard band limit (Δ_1+ Δ_2) of 10%.

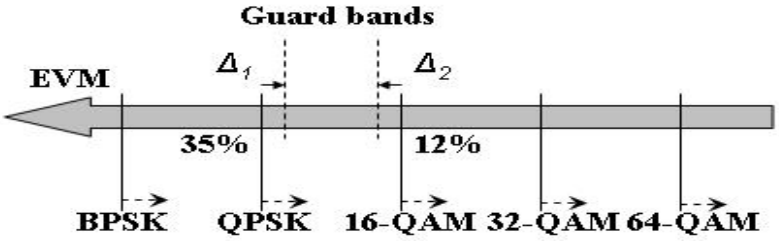


Figure 115 Exploiting the EVM margins for each data rate

4.5.3 Hardware Test Setup and Evaluation

Figure 116 plots the measured power consumption levels in RF receiver under different channel conditions for EVM specification compliance of 30% (including guard band limits) for QPSK modulation. Adaptive LNA and mixer modules were designed using off-the-shelf transistors and other components on FR-4 for evaluation purposes. The supply and bias was voltages were controlled using precision DC power supply

sources with GPIB control from the PC. The OFDM baseband functionality was coded in the PC and is interfaced with the RF front-end through National Instruments DAQ card. Different channel conditions were simulated by the addition of noise source and attenuation in RF path between the transmitter and receiver.

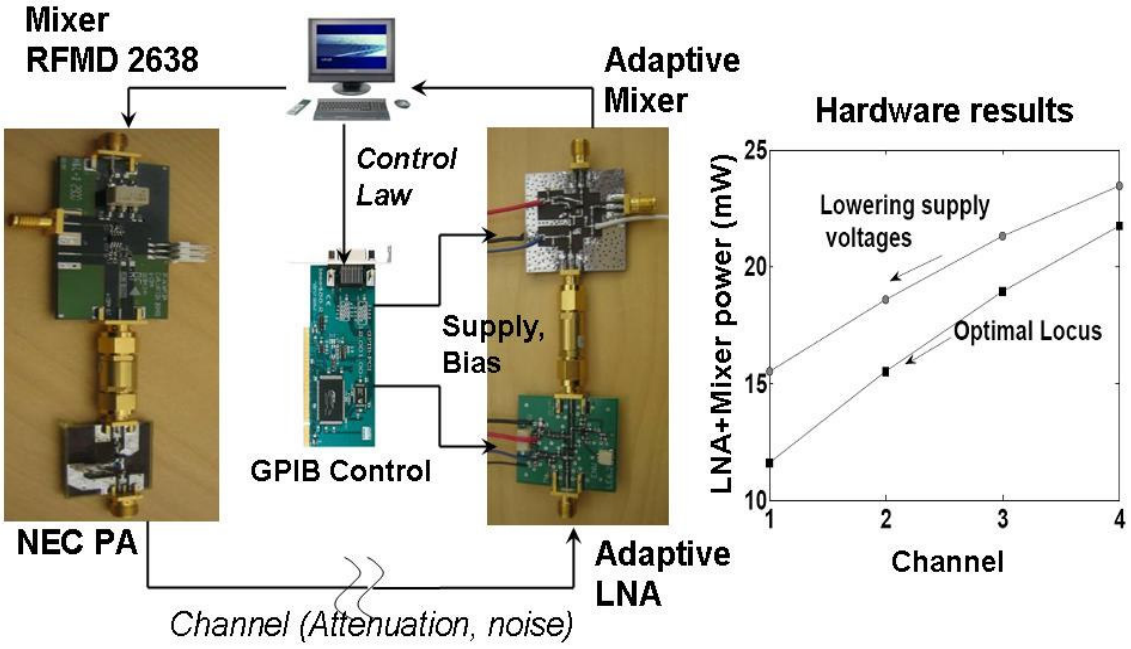


Figure 116 Hardware test setup and measurement results: RF power consumption with and without the optimal control law.

Experiments were performed to obtain the optimal power consumptions for four different moderate channel conditions. The system was first tested only the supply voltage as the control knob. Later, the optimal control law (that changes both the supply and bias based on the locus) was used to adapt the system. For both the cases, the receiver was operated at the EVM threshold for QPSK. It is observed from Figure 116 that greater power saving is obtained when RF front-end is operated along the *optimal locus* for all the channels. This proves that need for multidimensional adaptation and control for obtaining maximum savings in power.

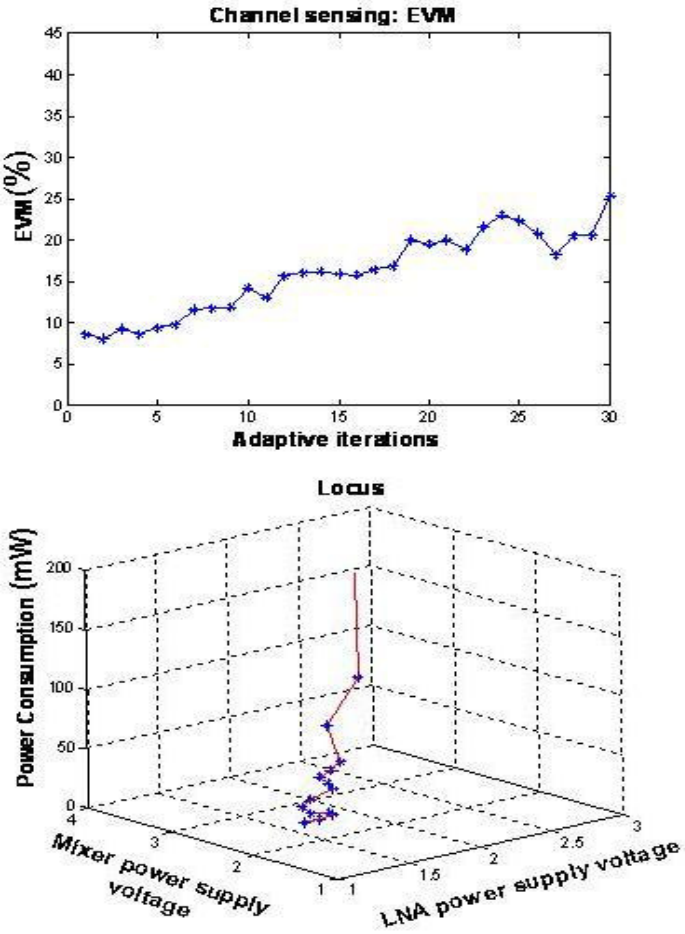


Figure 117 Run time operation of the VIZOR receiver: EVM and power adaptations for QPSK modulation

Dynamic adaptation of the receiver for reduced power consumption is observed in Figure 117. The figure plots the dynamically changing EVM and power consumption of the system for a particular channel condition. As seen in the plots, when is system is turned on, it operates the various components at nominal power consumption. As the adaptation is turned on, the control law (implemented in the PC) starts to reduce the receiver power consumption based on the optimal control law (locus) stored in the PC. During adaptation, EVM is dynamically computed to ensure that it stays below a fixed value. In this case, QPSK modulation was employed and the corresponding threshold

BER was set at 35%. As observed in the plots, with each iteration, the power consumption of the EVM is received and the corresponding EVM value increases. This continues until EVM reaches the threshold, after which, the system hovers around that point. The system remains in this until there is a change in the channel conditions, after which it adapts to reach the new optimum operating point.

The proposed multi-dimensional adaptation can be extended to include multiple control knobs (ADC word size, and sampling rate etc.) leading to a comprehensive system-level optimization problem. The software/hardware and power overhead for implementing the proposed feedback control must be considered carefully. The proposed approach is effective in increasing the battery life of the future multi-mode, multi-standard radios with multiple RF front-ends and power hungry DAC/ADCs, while consuming relatively little power and software/hardware overheads. The design of the power control circuitry is crucial in the proposed approach, as it determines the power savings that can be obtained under varying channel conditions. Under fast varying channel conditions, low-power operability would be limited by the response and settling time of the feedback control circuitry.

In conclusion, this chapter presented a multi-dimensional approach for dynamic adaptation of a wireless device for reduced power consumption without violating system-level performance metrics. The proposed approach aggressively exploits the built-in margins in wireless systems to enable minimum power operation. The framework was implemented on an OFDM RF receiver system and analyzed under different channel conditions.

Chapter 5

CONCLUSIONS AND FUTURE WORK

Low-cost test, diagnosis and tuning techniques for wireless devices were presented in this thesis. The proposed methodologies enable reduction of product development costs, and increased reliability of devices in the field. The proposed techniques are employed either during the manufacturing phase or during field operation. Later, a test-enabled low power adaptation framework for wireless receivers was discussed. The proposed framework uses a multidimensional control law to dynamically tune the device for reduced power operation while maintaining system-level performance specifications. The enable tuning, the supply and bias voltages of the LNA and mixer modules and ADC word size were used as the control knobs. An optimal control law implemented in the DSP tuned the control knobs for optimal power consumption under all conditions.

Further enhancements of the proposed framework can utilize additional control knobs such as sampling rate, feedback control mechanisms between the transmitter and receiver that enable the operation at minimum power level necessary for maintaining communication. The work presented in thesis primarily dealt with tuning the circuit components of a wireless receiver. A comprehensive framework that includes both the transmitter and receiver is necessary to realize the complete potential of the proposed approach, thereby, significantly increasing the battery life of the device. This would require the optimization over multiple levels and a more complex feedback control law.

Efficiency of the proposed approach is increased if the test and diagnosis is performed at different design levels across circuit, architecture, protocol, and application layer.

For future sub 45nm CMOS technologies and beyond, with dense integration for multi-mode circuits on-chip, the manufactured circuits are expected to be increasingly susceptible process variations along with other effects such as signal coupling, ground bounce, noise. This inherent process variability can cause the multi-dimensional control (discussed in this thesis) developed for one device unsuitable for application in another device. Novel techniques are required to address the above problem. In particular, carefully designed test and diagnosis procedures are used to first diagnose subsystem (module) level performance vs. power vs. reliability is necessary. The diagnostic information generated should then be used to dynamically optimize (post-manufacture) module level behavior in a highly nonlinear but near-continuous space to optimize system level performance, power and reliability metrics via specially designed hardware and software control mechanisms. The test complexity, the diagnostic data, and the complexity of diagnosis will be commensurate with the degree of adaptability (number of design control parameters) at each design level and needs to be designed to provide just the "right" amount of information to enable zero or near-zero-margin operation at that level of the design. This test-driven adaptability can then be used to maximize manufacturing yield and minimize field failures through built-in test driven monitoring of electrical wear out mechanisms and minimize product cost.

REFERENCES

[1] S. R. Nassif, “Modeling and analysis of manufacturing variations,” In *Proc. IEEE Conf. on Custom Integrated Circuits, 2001*, pp. 223-228.

[2] S. R. Nassif, “Design for variability in DSM technologies,” in *Proc. Int. Symp. Quality Electronic Design*, 2000, pp. 451-455.

[3] J. Turino, “Test economics in the 21st century,” *IEEE Design & Test*, vol. 14, pp. 41-44, 1997.

[4] R. Kramer, “Test throughput for mixed-signal devices,” *IEEE Instrumentation and Measurement Mag.*, vol. 8, pp. 12-15, 2005.

[5] ITRS public document “International Technology Roadmap for Semiconductors - 2004 update – Test and Test Equipment.”

[6] M. Slamani, "Reducing high-speed/RF test cost - guaranteed by design or guaranteed to fail?," *IEEE International Test Conference*, Austin, TX, USA, 2006, pp. 1.

[7] Keith B. Schaub and Joe Kelly, “Production Testing of RF and System-on-a-Chip Devices for Wireless Communications,” Artech House, Boston, 2004, Chapters 1 and 3.

[8] Agilent PN 89400-14 Product note, “Using Error Vector Magnitude Measurements to Analyze and Troubleshoot Vector-Modulated Signals, “Agilent Technologies, Santa Clara, USA.

[9] K. Voelker, "Apply error vector measurements in communications design," *Microwaves & Amp*; RF, vol. 34, pp. 143-4, 1995.

[10] R. Williams and J. Getchell, "High-speed measurement of digital wireless system SNR by means of error vector magnitude analysis," *Proceedings Wireless Communications Conference*, Boulder, CO, USA, 1996, pp. 68-70.

[11] S. Bhattacharya, R. Senguttuvan, and A. Chatterjee, "Production test enhancement techniques for MB-OFDM ultra-wide band (UWB) devices: EVM and CCDF," *IEEE International Test Conference*, Austin, TX, USA, 2006, p. 10 pp.

[12] "IEEE standard test access port and boundary-scan architecture", IEEE Std 1149.1-2001.

[13] "IEEE standard for a mixed-signal test bus", IEEE Std 1149.4-1999.

[14] S. Sunter, "The P1149.4 mixed signal test bus: Costs and benefits," Proc. Int. Test Conf., 1995, pp. 444–450.

[15] K. Lofstrom, "Early capture for boundary scan timing measurements", Proc. Int'l Test Conf., 1996, pp. 417-422.

[16] M. Mendez-Rivera, J. Silva-Martinez, E. Sánchez-Sinencio, "On-chip spectrum analyzer for built-in testing analog ICs," *Proceedings of International Symposium. on Circuits and Systems*., 2002, vol. 5 , pp. 61-64.

[17] A. Hajjar and G. W. Roberts, "A high speed and area efficient on-chip analog waveform extractor", *Proc. Int'l Test Conf.*, 1998, pp. 688–697.

[18] M. M. Hafed, N. Abaskharoun and G. W. Roberts, "A 4-GHz effective sample rate integrated test core for analog and mixed-signal circuits," *IEEE Trans. Solid State Circuits*, vol. 37, Apr 2002, pp. 499-514.

[19] B. R. Veillette and G. W. Roberts, "A built-in self-test strategy for wireless communication systems," *Proc. Int'l Test Conf.*, 1995, pp. 930-939.

[20] J. Dabrowski and J. G. Bayon, "Mixed loopback BiST for RF digital transceivers," Proceedings 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Cannes, France, 2004, pp. 220-8.

[21] S. Ozev, A. Orailoglu and H. Haggag, "Automated test development and test time reduction for RF subsystems," *IEEE Intl. Symp. on Circuits and Sys.,* 2002, pp. 581-584.

[22] S. Ozev, C. Olgaard and A. Orailoglu, "Testability implications in low-cost integrated radio tranceivers: A Bluetooth case study," *Proc. Int'l Test Conf.*, 2001, pp. 965-974.

[23] E. L. Crow and M. J. Miles, "A minimum cost, accurate statistical methods to measure bit error rates," *Proc. Int'l Council Computer Comm. Conf.*, 1976, pp. 631-635.

[24] M. C. Jeruchim, "Techniques for estimating the bit error rate in the simulation of digital communication systems," *IEEE J. Select. Areas Comm.*, vol. SAC-2, no. 1, 1984, pp. 153-170.

[25] R. Illasun, M. Flaherty, R. Matreci and M. Taylor, "Effective Evaluation of Link Quality using Error Vector Magnitude Techniques," *Proc. Wireless Comm. Conf.*, 1998, pp. 89-94.

[26] F. Lin, S. Chen and H. Chuang "Computer simulation of nonlinear effects of RF power amplifiers based on EVM and ACPR for digital wireless communications," *Electronic Letters*, Jan 2000, pp. 77-79.

[27] S. M. Berber, "An Automated Method of BER Characteristics Measurement," *Trans. Instrumentation and Measurement*, vol. 53, no. 2, Apr 2004, pp. 575-580.

[28] P. Palacharla, J. Chrostowski, R. Neumann and R. J. Gallenberger, “Techniques for Accelerated Measurement of Low Bit Error Rates in Computer Data Links,” *Proc. Int’l Phoenix Conf.*, 1995, pp. 184-190.

[29] M. S. Berber, “A time efficient method for bit error rate measurement,” *Proc. Asia-Pacific Conf. Comm.*, 2000, pp. 401-405.

[30] M. Helfenstein, E. Baykal, K. Muller, and A. Lampe, "Error vector magnitude (EVM) measurements for GSM/EDGE applications revised under production conditions," *IEEE International Symposium on Circuits and Systems*, Kobe, Japan, 2005, vol. 5, pp. 5003-5006.

[31] L. H. Tran, T. Mai, and J. A. Molnar, "Matlab and COTS instrumentations to reduce time and risk factors in design to the stand-alone QAM test system," *IEEE Systems Readiness Technology Conference*, Anaheim, CA, USA, 2003, pp. 490-495.

[32] A. Halder and A. Chatterjee, "Low-cost production testing of wireless transmitters," *Proceedings of 19th International Conference on VLSI Design*, Hyderabad, India, 2006, pp. 6-8.

[33] P.N. Variyam, S. Cherubal, and A. Chatterjee, “Prediction of analog performance parameters using fast transient testing,” *IEEE Trans. Computer-Aided Design*, vol. 21, pp. 349-361, 2002.

[34] A. Haldar, S. Bhattacharya, and A. Chatterjee, “Automatic multitone alternate test generation for RF circuits using behavioral models,” In *Proc. Int. Test Conf.*, 2003, pp. 665-673.

[35] R. Voorakaranam, S. Cherubal and A. Chatterjee, “A Signature Test Framework for Rapid Production Testing of RF Circuits,” Proc. Design Automation and Test in Europe, 2002, pp. 186 - 191.

[36] S. S. Akbay and A. Chatterjee, "Feature Extraction Based Built-In Alternate Test of RF Components Using a Noise Reference," *Proc. VLSI Test Symp.,* 2004, pp. 273-278.

[37] G. Srinivasan, S. Bhattacharya, S. Cherubal and A. Chatterjee, "Efficient Test Strategy for TMDA Power Amplifiers Using Transient Current Measurements: Uses and Benefits," *Proc. Design Automation and Test in Europe*, 2004.

[38] Nikhil Despande, et al, “ACPR Specs Place Demands on WCDMA Base-Station Amplifiers,” Wireless Systems Design Magazine, Aug 1999, pp. 15-22.

[39] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High-speed Physical Layer in the 5 GHz Band, IEEE std P802.11a-1999.

[40] ETSI TS 101 475 V1.2.1A, Broadband Radio Access Networks (BRAN); HIPERLAN Type 2; Physical (PHY) layer, April 2000.

[41] B. Razavi, *RF Microelectronics*. Prentice Hall, New Jersey, 1998.

[42] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press, 2002.

[43] D.Han, S.S. Akbay, S. Bhattacharya, A. Chatterjee, W.R. Eisenstadt, “On-chip self-calibration of RF circuits using specification-driven built-in self test (S-BIST), *Proceedings of 11th International On-line Testing Symposium*, July 2005, pp. 106-111.

[44] O. Jeon, R.M. Fox, B.A. Myers, “Analog AGC Circuitry fro a CMOS WLAN Receiever”, *IEEE Journal of Solid-State Circuits,* Volume 41, Issue 10, Oct 2006, pp 2291-2300.

[45] M. Neuhauser, M. Moller, M. Rein, H. Wernz, “ Low-noise, high-transimpedance Si-bipolar AGC amplifier for 10Gb/s optical-fiber links”, *IEEE Photonics Technology Letters,* Volume 7, Issue 5, May 1995, pp. 549-551.

[46] B.S. Song, P.R. Gray, “A Precision curvature-compensated CMOS bandgap reference”, *IEEE Jour nal of Solid-State Circuits*, Volume 18, Issue 6, Dec 1983, pp. 634-643.

[47] E.A.Vittoz, O. Neyroud, “A low-voltage CMOS bandgap reference”, *IEEE Journal of Solid-State Circuits*, Volume 14, Issue 3, Jun 1979, pp. 573-579.

[48] J.K. Cavers, M.W. Liao, “Adaptive Compensation for Imbalance and Offset Losses in Direct Conversion Transceivers”, *IEEE Transactions on Vehicular Technology,* Volume 42, Issue 4, November, 1993, pp. 581-588.

[49] C.H. Park, J.H. Paik, Y-H You, M-C Ju, J-W Cho, “ Techniques for Channel Estimation , DC-offset Compensation, and Link Quality Control in Bluetooth System”, *IEEE Transactions on Consumer Electronics*, Volume 46, Issue 3, August 2000, pp. 682-689.

[50] I. Elahi, K. Muhammad, P.T Balsara, “I/Q Mismatch compensation using Adaptive Decorrelation I a Low-IF Receiver in 90-nm CMOS Process”, *IEEE Journal of Solid-State Circuits*, Vol. 41, Issue 2, February, 2006, pp. 395-404.

[51] M. Valkama, K. Salminen, M. Renfors, "Digital I/Q Imbalance Compensation in Low-IF Receivers: Principles and Practice, *14th International Conference on Digital Signal Processing*, Volume 2,July 2002, pp. 1179-1182.

[52] P. Capozio, P. Pai, E. Vizzi, G. Dacosta, "A Novel adaptive technique for digital I/Q imbalance compensation in OFDM receivers", *Proceedings of IEEE International Conference on Acoustics, Speech and Signal Processing*, Volume 3, March 2005, pp. 817-820.

[53] P. Rykaczewki, D. Pienkowski, R. Cadu, B. Steinke, "Signal Path Optimization in Software-Defined Radio Systems", *IEEE Transactions on Microwave Theory and Techniques,* Volume 53, Issue 3, March 2005, pp. 1056-1064.

[54] G-J Van Rooyen, J.G. Lourens, "Non-Iterative Compensation for Software-Defined Radio Quadrature Front-end Inaccuracies", *Proceedings of Wireless Communications, Networking and Mobile Computing*, Volume 1, September 2005, pp. 598-601.

[55] S. Lee, S. Das, T. Pham, T. Austin, D. Blaauw and T. Mudge, "Reducing Pipeline Energy Demands with Local DVS and Dynamic Retiming," Proceedings of the ISLPED'04, Aug 2004, pp: 319-324.

[56] D. Ernst, S. Das, S. Lee, D. Blaauw, T. Austin, T. Mudge, N. S. Kim, K. Flautner, "RAZOR: Circuit-Level Correction Of Timing Errors For Low-Power Operation," IEEE Micro, Vol. 24, Issue 6, Nov-Dec 2004 pp:10 – 20.

[57] D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, C. Ziesler, D. Blaauw, T. Austin, K. Flautner and T. Mudge, "Razor: A Low-Power Pipeline Based on Circuit-

Level Timing Speculation," Proceedings of the 36th International Symposium on Microarchitecture (MICRO-36'03), pp: 7 – 18.

[58] Burd, T.D., Pering, T.A., Stratakos, A.J., Brodersen, R.W., "A dynamic voltage scaled microprocessor system," IEEE Journal of Solid-State Circuits, Volume 35, Issue 11, Nov. 2000 Page(s):1571 – 1580.

[59] Abidi, A., Pottie, G.J., Kaiser, W.J., "Power-conscious design of wireless circuits and systems", Proceedings of the IEEE, vol 88,Issue 10, Oct 2000, pp. 1528-1545.

[60] A. N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and Mixer," IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1939-1944.

[61] C. Y. Wu and H. S. Kao, "A 2-V Low-Power CMOS Direct-Conversion Quadrature Modulator With Integrated Quadrature Voltage-Controlled Oscillator and RF Amplifier for GHz RF Transmitter Applications," IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 49, No. 2, February 2002, pp. 123-134.

[62] T. Kawamura, M. Suzuki and H. Ichino, "An Extremely Low-power Bipolar Current-mode 1/0 Circuit for Multi-Gbit/s Interfaces," Proceedings of 1994 Symposium on VLSl, June 1994, pp: 31-32.

[63] S.K. Kim, Y.-S. Son and G.H. Cho, "Low-power high-slew-rate CMOS buffer amplifier for flat panel display drivers," IEEE Electronics Letters, Volume 42, Issue 4, Feb. 2006, pp.214 – 216.

[64] B. G. Perumana, S. Chakraborty, C. H. Lee,and J. Laskar, "A Fully Monolithic 260-_W, 1-GHz Subthreshold Low Noise Amplifier," IEEE Microwave And Wireless Components Letters, Vol. 15, No. 6, June 2005, pp. 428-430.

[65] Tasic, A., Lim, Su-Tarn, Serdjin, W.A., Long, J.R., "Design of Adaptive Multi-mode RF Front-end Circuits", IEEE Journal of Solid State Circuits, Vol. 42, No. 2, Feb 2007.

[66] Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, Z. Lu, "A novel CMOS low-noise amplifier design for 3.1- to 10.6-GHz ultra-wide-band wireless receivers," IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 53, No. 8, August 2006, pp. 1683 – 1692.

[67] H.Woesner, J.P. Ebert, M. Schlager, and A. Wolisz, "Power saving mechanisms in emerging standards for wireless LANs: The MAC layer perspective", IEEE Personal Communication Systems, 5(3): 40-48, 1998.

[68] Tasic, A., Serdjin, W.A., Long, J.R., "Adaptive multi-standard ciruits and systems for wireless communications", IEEE Circuits and Systems Magazine, Vol 6., Issue 1., pp. 29-37.

[69] Brodersen, B. etal., "Wireless systems-on-a-chip design", 2002. Proceedings. International Symposium on Quality Electronic Design, 18-21 March 2002 Page(s):221.

[70] Brodersen, R.W.; Davis, W.R.; Yee, D.; Ning Zhang; "Wireless systems-on-a-chip design", 2001 International Symposium Proceedings of VLSI Technology, Systems, and Applications, 18-20 April 2001 Page(s):45 – 48.

[71] Melly, T.; Porret, A.-S.; Enz, C.C.; Vittoz, E.A., "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: transmitter", IEEE Journal of Solid-State Circuits, Volume 36, Issue 3, March 2001 Page(s):467 – 472.

[72] Debaillie, B. Bougard, B., Lenoir, G., Vandersteen G., Catthoor, F., “Energy-scalable OFDM transmitter design and control”, 43rd IEEE Design Automation Conference, July 24-28, pp. 536-541.

[73] D.Porcino, W.Hirt, "Ultra-wideband radio technology: potential and challenges ahead," Communications Magazine, IEEE, Volume: 41, Issue: 7, July 2003, pp. 66 – 74.

[74] L.D.Paulson, "Will ultrawideband technology connect in the marketplace?" Computer, Volume: 36, Issue: 12, Dec. 2003, pp. 15 – 17.

[75] G.R.Aiello, G.D.Rogerson, “Ultra-wideband wireless systems”, IEEE Microwave Magazine, Volume 4, Issue 2, June 2003, pp. 36 – 47.

[76] Multiband OFDM Alliance: http://www.multibandofdm.org/, April, 2007.

[77] The International Engineering Consortium (IEC) Web ProForum Tutorials, “OFDM for Mobile Data Communications”, http://ww.iec.org, Jan 2007.

[78] Batra, A., “Achieving High Speed Wireless Communications Using a Multi-Band OFDM UWB System” Ultrawideband Radio Communications, ISCAS, May 2004.

[79] IEEE proposal “Multi-band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a”, Document Number P802.15-03/268r3, March 2004.

[80] Marc Engels, *Wireless OFDM Systems*, Kluwer Academic Publishers, Boston, 2003.

[81] Bhattacharya, R. Senguttuvan, and A. Chatterjee, "Production test enhancement techniques for MB-OFDM ultra-wide band (UWB) devices: EVM and CCDF," IEEE International Test Conference, Austin, TX, USA, 2006, p. 10 pp.

[82] Mathworks Inc., MATLAB/Simulink software, www.mathworks.com, Dec 2004.

[83] Altera Corporation, “Stratix-II Development Kit”, San Jose, California, USA.

[84] Godara, B., Blamon, G., and Fabre, A., "UWB : A New Efficient Pulse Shape and its Corresponding Simple Transceiver," 2nd International Symposium on Wireless Communication Systems, 2005., 5-7 Sept. 2005 , pp. 365- 369.

[85] Krishnan, S., Kyaw, O., Low Zhen Ning, Kumar, V.P., and Leng, N.L., "Tunable monocycle doublet generator," 2006 IEEE Radio and Wireless Symposium, 17-19 Jan., 2006, pp. 387- 390.

[86] Shpak,V.G., Oulmascoulov, M.R., Shunailov, S.A., and Yalandin, M.I., "Active former of monocycle high-voltage subnanosecond pulses," *12th IEEE International Pulsed Power Conference Digest of Technical Papers*, 1999, vol.2, pp.1456-1459.

[87] Buchegger, T., Ossberger, G., Reisenzahn, A., Stelzer, A., and Springer, A., "Pulse delay techniques for PPM impulse radio transmitters," *2003 IEEE Conference on Ultra Wideband Systems and Technologies*, 16-19 Nov., 2003, pp. 37- 41.

[88] Jeongwoo Han, and Cam Nguyen, "Ultra-wideband electronically tunable pulse generators," *IEEE Microwave and Wireless Components Letters, [see also IEEE Microwave and Guided Wave Letters]*, vol.14, no.3, March 2004, pp. 112- 114.

[89] Jeongwoo Han, and Cam Nguyen, "Coupled-slotline-hybrid sampling mixer integrated with step-recovery-diode pulse generator for UWB applications," *IEEE Transactions on Microwave Theory and Techniques,* vol.53, no.6, June 2005, pp. 1875-1882.

[90] Jeongwoo Han, and Nguyen, C., "On the development of a compact sub-nanosecond tunable monocycle pulse transmitter for UWB applications," IEEE Transactions on Microwave Theory and Techniques, vol.54, no.1, Jan. 2006, pp. 285-293.

[91] Krishnan, S., Kyaw, O., Low Zhen Ning, Kumar, V.P., and Leng, N.L., "Tunable monocycle doublet generator," *2006 IEEE Radio and Wireless Symposium*, 17-19 Jan., 2006, pp. 387- 390.

[92] Pepper, S.H., Sr., "Quadrature/correlating sampler and pulse generator for mmwave UWB QAM modulation and wide-band signaling," *2005 European Microwave Conference*, vol.3, 4-6 Oct. 2005, pp. 3.

[93] Rulikowski, P., and Barrett, J., "Truly balanced step recovery diode pulse generator with single power supply," *2004 IEEE Radio and Wireless Conference*, 19-22 Sept., 2004, pp. 347- 350.

[94] Yilmaz, S., and Tekin, I., "Ultra-wideband n-bit digitally tunable pulse generator," *2005 IEEE International Conference on Ultra-Wideband*, 5-8 Sept. 2005, pp. 438- 441.

[95] Jeong Soo Lee, and Cam Nguyen, "Novel low-cost ultra-wideband, ultra-short-pulse transmitter with MESFET impulse-shaping circuitry for reduced distortion and improved pulse repetition rate," *IEEE Microwave and Wireless Components Letters [see also IEEE Microwave and Guided Wave Letters]* , vol.11, no.5, May 2001, pp.208-210

[96] Jeong-Woo Han, Meng Miao, and Cam Nguyen, "Recent development of SRD- and FET-based sub-nanosecond pulse generators for ultra-wideband communications," *2003. IEEE Topical Conference on Wireless Communication Technology*, 15-17 Oct. 2003, pp. 441- 442.

[97] Gill, G. S., Chiang,H. F., and Hall,J., "Waveform synthesis for ultra wideband radar," *Record of the 1994 IEEE National Radar Conference*, 1994, pp.240-245.

[98] Gill, G. S., "Ultra-wideband radar using Fourier synthesized waveforms," *IEEE Transactions on Electromagnetic Compatibility*, vol. 39, 1997, pp. 124-131.

[99] Keren Li, Kurita, D., and Matsui, T., "A novel UWB bandpass filter and its application to UWB pulse generation," 2005 *IEEE International Conference on Ultra-Wideband*, 5-8 Sept. 2005, pp. 446- 451.

[100] Adrian Eng-Choon Tan, Chia, M.Y.-W., and Leong, S.-W., "Sub-nanosecond pulse-forming network on SiGe BiCMOS for UWB communications," *IEEE Transactions on Microwave Theory and Techniques*, vol.54, no.3, March 2006, pp. 1019- 1024.

[101] Azakkour, A., Regis, M., Pourchet, F., and Alquie, G., "A new integrated monocycle generator and transmitter for ultra-wideband (UWB) communications," *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, 12-14 June 2005, pp. 79-82.

[102] Bagga, S., de Vita, G., Haddad, S.A.P., Serdijn, W.A., and Long, J.R., "A PPM Gaussian pulse generator for ultra-wideband communications," *Proceedings of the 2004 International Symposium on Circuits and Systems*, 23-26 May 2004, vol.1, pp. I-109- I-112.

[103] Bagga, S., Serdijn, W.A., and Long, J.R., "A PPM Gaussian monocycle transmitter for ultra-wideband communications," *2004 International Workshop on Ultra Wideband Systems - Joint with Conference on Ultrawideband Systems and Technologies*, 18-21 May 2004, pp. 130- 134.

[104] Hyunseok Kim, Dongwon Park, and Youngjoong Joo, “Design of CMOS Scholtz's monocycle pulse generator,” *2003 IEEE Conference on Ultra Wideband Systems and Technologies*, 16-19 Nov. 2003, pp. 81- 85.

[105] Jeongwoo Han, and Cam Nguyen, “A new ultra-wideband, ultra-short monocycle pulse generator with reduced ringing,” *IEEE Microwave and Wireless Components Letters, [see also IEEE Microwave and Guided Wave Letters]*, vol.12, no.6, Jun 2002, pp.206-208.

[106] Junwoo Lee, Young-Jin Park, Myunghoi Kim, Yoon, C., Joungho Kim, and Kwan-Ho Kim, “System-on-package ultra-wideband transmitter using CMOS impulse generator,” *IEEE Transactions on Microwave Theory and Techniques*, vol.54, no.4, June 2006, pp. 1667- 1674.

[107] Marsden , K., Hyung-Jin Lee, Dong Ha, and Hyung-Soo Lee, “Low power CMOS re-programmable pulse generator for UWB systems,” *2003 IEEE Conference on Ultra Wideband Systems and Technologies*, 16-19 Nov. 2003, pp. 443- 447.

[108] Norimatsu, T., Fujiwara, R., Kokubo, M., Miyazaki, M., Ookuma, Y., Hayakawa, M., Kobayashi, S., Koshizuka, N., and Sakamura, K., “A novel UWB impulse-radio transmitter with all-digitally-controlled pulse generator,” *Proceedings of the 31st European Solid-State Circuits Conference*, 12-16 Sept. 2005, pp. 267- 270.

[109] O'Donnell, I.D., and Brodersen, R.W., “An ultra-wideband transceiver architecture for low power, low rate, wireless systems,” IEEE Transactions on Vehicular Technology, vol.54, no.5, Sept. 2005, pp. 1623- 1631.

[110] Saha, P.K., Sasaki, N., and Kikkawa, T., “A CMOS UWB transmitter for intra/inter-chip wireless communication,” *2004 IEEE Eighth International Symposium on Spread Spectrum Techniques and Applications*, 30 Aug.-2 Sept. 2004, , pp. 962- 966.

[111] Kevin M. Marsden, "A Study of a Versatile Low Power CMOS Pulse Generator for Ultra Wideband Radios," Virginia Polytechnic Institute and State University, *Thesis for Master of Science*, 2003.

[112] Blazquez, R., Newaskar, P.P., Lee, F.S., and Chandrakasan, A.P., “A baseband processor for pulsed ultra-wideband signals,” *Proceedings of the IEEE Custom Integrated Circuits Conference*, 3-6 Oct. 2004, pp. 587- 590

[113] Chao Fang, Yuanjin Zheng, and Choi Look Law, “An ultra wideband transmitter based on up conversion architecture,” Proceedings of 2005 IEEE International Workshop on Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks, 30 Nov.-2 Dec. 2005, pp. 4

[114] Demirkan, M., and Spencer, R.R., “A low-sensitivity on-chip impulse radio pulse generation method,” *Conference Record of the Thirty-Eighth Asilomar Conference on Signals, Systems and Computers*, vol.1, 7-10 Nov. 2004, pp. 1020- 1024

[115] Wentzloff, D.D., and Chandrakasan, A.P., “A 3.1-10.6 GHz ultra-wideband pulse-shaping mixer,” *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium Digest of Papers*, 12-14 June 2005, pp. 83- 86.

[116] Shen, M., Koivisto, T., Peltonen, T., Zheng, L.-R., Tjukanoff, E., and Tenhunen, H., “UWB transceiver circuits design for WPANs applications,” *International Symposium on Signals, Circuits and Systems*, vol.1, 14-15 July 2005., pp. 255- 258.

[117] Shen, M., Koivisto, T., Peltonen, T., Zheng, L.-R., Tjukanoff, E., and Tenhunerf, H., "UWB radio module design for wireless sensor networks," *23rd NORCHIP Conference*, 21-22 Nov. 2005, pp. 184- 187.

[118] Dilmaghani, R.S., Ghavami, M., and Aghvami, A.H., "UWB multiple-pulse generator and transmitter," *2004 International Workshop on Ultra Wideband Systems and Technologies*, 18-21 May 2004, pp. 117- 121.

[119] Kim, H., Park, D., and Joo, Y., "All-digital low-power CMOS pulse generator for UWB system," *IEEE Electronics Letters*, vol.40, no.24, 25 Nov. 2004, pp. 1534- 1535

[120] Luyong Zhang, Zheng Zhou, "A novel synthesis design and implementation for generating UWB narrow pulse based on wavelet*," IEEE International Symposium on Communications and Information Technology*, vol.2, 26-29 Oct. 2004, pp. 1228- 1231

[121] Yun Hwa Choi, "Gated UWB pulse signal generation," *2004 International Workshop on Ultra Wideband Systems,* 18-21 May 2004, pp. 122- 124

[122] Zimmer, R., Waldow, P., and Beyer, A., "An improved method of generating UWB pulses for high datarate communication," *2006 IEEE Radio and Wireless Symposium*, 17-19 Jan. 2006, pp. 143- 145.

[123] Agilent application note "Characterizing Digitally Modulated Signals with CCDF Curves", Available at www.agilent.com., Apr 2007.

[124] C. Hsin-Hung, L. Chih-Hung, H. Po-Chiun, and C. Jiunn-Tsair, "Joint polynomial and look-up-table predistortion power amplifier linearization," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 53, pp. 612-16, 2006.

[125] P. In-Seung, E. J. Powers, and X. Guanghan, "Parallel adaptive predistortion for RF power amplifier linearization," in GLOBECOM 97. *IEEE Global Telecommunications Conference*, Phoenix, AZ, USA, 1997, pp. 82-6.

[126] M. Isaksson, D. Wisell, and D. Ronnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 348-59, 2006.

[127] W. J. Kim, K. J. Cho, S. P. Stapleton, and J. H. Kim, "Baseband derived RF digital predistortion," *Electronics Letters*, vol. 42, pp. 468-70, 2006.

[128] B. M. Lee and R. J. P. de Figueiredo, "Adaptive predistorters for linearization of high-power amplifiers in OFDM wireless communications," *Circuits, Systems, and Signal Processing*, vol. 25, pp. 59-80, 2006.

[129] O. Leulescu and T. Petrescu, "Nonlinear predistortion for dynamic power amplifiers linearization," in 2005 *European Conference on Wireless Technologies*, Paris, France, 2006, pp. 333-6.

[130] M. O'Droma, E. Bertran, M. Gadringer, S. Donati, A. Zhu, P. L. Gilabert, and J. Portilla, "Developments in predistortion and feedforward adaptive power amplifier linearisers," in 2005 *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, Paris, France, 2006, pp. 337-40.

[131] Y. Qian, Q. Li, and T. Yao, "Analysis of different predistortion structures and efficient least-square adaptive algorithms," in *2003 IEEE International Conference on Acoustics, Speech, and Signal Processing*, Hong Kong, China, 2003, pp. 461-4.

[132] Hilborn, D.S, Stapleton, S.P., J.K. Cavers, “An adaptive direct conversion transmitter”, *IEEE Transactions on Vehicular Technology*, vol. 43, issue 2, May 1994, pp. 223-233.

[133] G. Orengo, P. Colantonio, A. Serino, F. Giannini, G. Ghione, M. Pirola, and G. Stegmayer, "Time-domain neural network characterization for dynamic behavioral models of power amplifiers," in 2005 *13th European Gallium Arsenide and other Compound Semiconductors Application Symposium*, Paris, France, 2006, pp. 189-92.

[134] Z. Anding, J. Dooley, and T. J. Brazil, "Simplified Volterra series based behavioral modeling of RF power amplifiers using deviation-reduction," in 2006 *IEEE MTT-S International Microwave Symposium Digest*, San Francisco, CA, USA, 2006, pp.38-4.

[135] D. Han and A. Chatterjee, “Robust built-in test of RF ICs using envelope detectors,” *Asian Test Symposium*, pp. 2-7, 2005.

[136] California Eastern Laboratories data sheet on NESG2021, Santa Clara, CA.

[137] Skyworks Inc application note “Plastic Packaged Hyperabrupt Junction Silicon Chips,” Woburn, MA.

[138] Agilent application note “Diode Detector Simulation using Agilent Technologies EEsof ADS Software”, AN1187, 1999.

[139] Agilent technical datasheet, “Surface Mount Microwave Schottky Detector Diodes: HSMS-286x Series”, 2004.

[140] National Instruments Inc, “PCI-6110 Data Acquisition card”, Available at www.ni.com, Dec 2004.

[141] Senguttuvan, R., Bhattarcharya, S., Chatterjee, A., “Design Consideration and Effect of Manufacturing Process Variations on UWB Transceiver Specifications”, proceedings of ICU 2005, Zurich, pp 461-467.

[142] Artmi, Ltd., “Novel UWB Antennas – Theory and Simulation”, Applications and Notes, Sep 2002.

[143] C.L. Mak, K.M. Luk, K.F. Lee, “Wideband triangular patch antenna”, IEE Proc. Microwaves, Antennas and Propagation, Vol.146 (April 1999), pp. 167-168.

[144] Ultrawaves Inc., “Antenna Design, Analysis and Numerical Modeling for Impulse UWB,” White Paper, 2004.

[145] C. W. Kim et al., “An Ultra Wideband CMOS Low Noise Amplifier for 3-5 GHz UWB System”, *IEEE Journal of Solid-State Ciruits*, Vol. 40, No. 2, February 2005.

[146] L. Hsin-Piao and T. Ming Jian, "Analyzing GPS signals to investigate path diversity effects of non-geostationary orbit satellite communication systems," *International Journal of Satellite Communications*, vol. 20, pp. 435-54, 2002.

[147] Batra, A., “Achieving High Speed Wireless Communications Using a Multi-Band OFDM UWB System”, Ultrawideband Radio Communications, ISCAS, May 2004.

[148] B. Baggini, P. Basedau, R. Becker, P. Bode, R. Burdenski, F. Esfahani, W. Groeneweg, M. Helfenstein, A. Lampe, R. Ryter, and R. Stephan, "Baseband and audio mixed-signal front-end IC for GSM/EDGE applications," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1364-79, 2006.

[149] J. S. Min and H. Samueli, "Analysis and design of a frequency-hopped spread-spectrum transceiver for wireless personal communications," *IEEE Transactions on Vehicular Technology*, vol. 49, pp. 1719-31, 2000.

[150] Agilent Technologies Inc, “E4436B ESG-DP Series Digital RF Signal Generator“, Santa Rosa, California, 2005.

[151] Zhao, Y., Agee, B.G., Reed, J.H., “Simulation and measurement of microwave oven leakage for 802.11 WLAN interference management”, Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications, vol 2, Aug 8-12, 2005, pp.1580-1583.

[152] Yoshizawa, S., Miyanaga, Y., “Tunable wordlength architecture for a low power wireless OFDM demodulator”, IEICE Transaction Fundamentals, vol E89-A, No. 10, October 2006.